K.S.R. COLLEGE OF ENGINEERING, TIRUCHENCODE – 637 215
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
COURSE/ LESSON PLAN SCHEDULE
STAFF NAME: P. THILAGAVATHI
SUBJECT: 18EC314 - DIGITAL ELECTRONICS   **CLASS: II   B.E ECE**
A). TEXT BOOKS
1. M. Morris Mano, "Digital Design", 4th Edition, Prentice Hall of India Pvt. Ltd., 2012
2. Donald P.Leach and Albert Paul Malvino and Goutam Saha, "Digital Principles and Applications", McGraw Hill Education, 8th Edition 2015.
3. Charles H.Roth," Fundamentals of Logic Design",Thomson Learning, 5th Edition , 2011.
B). REFERENCE BOOKS
1John F.Wakerly, "Digital Design Principles and Practices", Pearson Education ,9th Impression, 2013.
2.John.M Yarbrough, "Digital Logic Applications and Design", Thomson Learning, 9 th Reprint, 2012.
3.Donald D.Givone, "Digital Principles and Design", Tata McGraw Hill, 21st Reprint , 2012.
4.Soumitra Kumar Mandal," Digital Electronic Principles and Applications", McGraw Hill,7th Reprint, 2014.
5.Stephen Brown, ZvonkoVranesic,"Fundamentals of Digital Logic with VHDL Design",TMH,3re Edition 2012.
6.NPTEL Course Link: http://nptel.ac.in/courses/117106086.
C). EXTRA REFERENCE BOOK
1. R.Ananda Natarajan,"DIGITAL DESIGN",PHI-2015.
D). LEGEND:

L 1	-	Lecture 1	BB	-	Block Board	Ex 1	-	Extra Ref Book 1
OHP	-	Over Head Projector	T 1	-	Tutorial 1	PPT	-	Power Point
Tx 1	-	Text Book 1	Rx 1	-	Reference Book 1	PP	-	Pages

S.NO	LECTURE HOUR	TOPICS TO BE COVERED	TEACHING AID REQUIRED	BOOK NO/PAGE NO
		UNIT I – MINIMIZATION TECHNIQUES AND LOGIC GATES		
1	L1	Boolean postulates and laws,De-Morgan's theorem, Principle of duality	BB	T_{X1}/pp 1-13, Tx2/pp 1- 25, Ex1/pp 1-25, Tx_3/pp 1-11
2	L2	Boolean expression, Minterm , Maxterm, Sum of Products, Product of Sums	BB	T_{X1}/pp 36-44, Ex1/pp 56-68, $Tx_{3/}$ pp 38-46
3	L3	Minimization of Boolean expression, Algebraic method	BB	T_{X1}/pp 44-57, Tx2/pp 46-55, Ex1/pp 68-70, Ex1/pp 85-88,
4	L4	Karnaugh map method, Don't care conditions	BB	T_{X1}/pp 70-87, Tx2/pp137-171, Ex1/pp 94-116, Tx_3/pp 109-144
5	L5	Quine-McCluskey method	BB	Ex1/pp 116-125, Tx2/pp 55-61, Tx_3/pp 109-44
6	L6	Logic gates: AND, OR, NOT, NAND, NOR, Exclusive-OR and Exclusive-NOR	PPT	T_{X1}/pp 55-60, Tx2/pp 55-61, Ex1/pp 70-74, Ex1/pp 88-89
7	L7	Implementations of Logic functions using gates	BB/PPT	T_{X1}/pp 87-94,E_{X1}/pp 86-88
8	L8	NAND-NAND,NOR-NOR implementations	BB/PPT	T_{X1}/pp 95-99, Tx2/pp 61-72, Ex1/pp 89-94
9	L9	TTL and CMOS digital logic families, Tristate Gates	BB/ OHP	T_{X1}/pp 512-518, T_{X1}/pp 172-174, Tx2/pp 61-72
		UNIT II – COMBINATIONAL CIRCUITS		
10	L10	Introduction,Design procedure, Half Adder, Full Adder, Half Subtractor, Full Subtractor	BB/ OHP	T_{X1}/pp 135, T_{X1}/pp 146, Tx2/pp 234-247,T_{X1}/pp 150-152, $Tx_{3/}$ pp 201-213, Ex1/pp 164-169,Ex1/pp 170-173
11	L11	Parallel Binary Adder, Parallel Binary Subtractor	BB/ OHP	T_{X1}/pp 146-147, Tx1/pp 152-155, Tx2/pp 246-247, Ex1/pp 169-170, Ex1/pp 173-175

12	L12	Fast Adder, Carry Look Ahead Adder	BB/ OHP	T_{X1}/pp147-150, Tx2/pp 244-245, Ex1/pp 175-177
13	L13	Serial Adder / Subtractor	BB/ OHP	T_{X1}/pp 258-261, Tx2/pp245-251
14	L14	BCD Adder	BB	T_{X1}/pp156-157,Ex1/pp 177-180
15	L15	Binary Multiplier, Binary Divider	BB	T_{X1}/pp158-159, Ex1/pp 180-182
16	L16	Code converters	BB/PPT	T_{X1}/pp 127-129, $Tx_{3/}$ pp 240-245, Ex1/pp 226-232, Tx2/pp 31-38
17	L17	Parity Generators, Parity Checker , Magnitude Comparator	BB	T_{X1}/pp 102-105,T_{X1}/pp 160-161, Tx2/p255-258, Tx2/pp 38-40, Ex1/pp 217-226,Ex1/pp233-235
18	L18	Decoders ,Encoders, Multiplexers and Demultiplexers	BB	T_{X1}/pp 146-158, $Tx_{3/}$ pp 235-238, Ex1/pp 204-217, Tx2/pp174190
		UNIT III – MEMORY AND PROGRAMMABLE LOGIC DEVICES		
19	L19	Classification of memories: ROM, PROM , EPROM , EEPROM , EAPROM, RAM	BB/PPT	T_{X1}/pp 313-314, Ex1/pp 489-502, Tx2/pp 486, Ex1/pp 505-516
20	L20	ROM - ROM organization - RAM - RAM organization	BB/PPT	T_{X1}/pp 322-324, T_{X1}/pp 308-311, Ex1/pp 492-495
21	L21	Memory expansion	BB/OHP	T_{X1}/pp 238-250, Tx2/pp 512-518, Ex1/pp 505-516
22	L22	Static RAM cell , Bipolar RAM cell , MOSFET RAM cell , Dynamic RAM cell	BB/OHP	T_{X1}/pp 328-332, Tx2/pp558-568, Ex1/pp 521-524
23	L23	Programmable Logic Devices - Programmable Logic Array (PLA)	BB	T_{X1}/pp 339-344, Tx2/pp 568-588,
24	L24	Programmable Array Logic (PAL) Field Programmable Gate Arrays (FPGA)	BB	T_{X1}/pp 332-336,
25	L25	Implementation of combinational logic circuits using ROM	BB	T_{X1}/pp 325-336, Ex1/pp 502-505,
26	L26	Implementation of combinational logic circuits using PLA	BB	Tx2/pp 490-500, Ex1/pp 521-530
27	L27	Implementation of combinational logic circuits using PAL	BB	Tx2/pp 490-500, Ex1/pp 521-530
		UNIT – IV SEQUENTIAL CIRCUITS		
28	L28	Latches and Flip flops : SR,JK,D ,T and Master-Slave flip-flops	BB/OHP	TX1/pp 199-210
29	L29	Characteristic table and equation, Application Table, Edge triggering and Level triggering	BB/OHP / PPT	TX1/pp 211-215
30	L30	Realization of one flip flop using other flip-flops	BB/OHP	T_{X1}/pp 233-246, Tx2/pp 283-289, Ex1/pp 384-406
31	L31	Asynchronous and Synchronous counter: Up, Down and Up/Down counters	BB	T_{X1}/pp 268-288, Tx2/pp 361-384, Ex1/pp 329-340,Ex1/pp 347-349
32	L32	Design of Synchronous counter	BB	Ex1/pp 349-364, Tx2/pp 319-346
33	L33	Modulo-n-counter	BB	Ex1/pp 341-345, Tx2/pp 361-384
34	L34	Shift registers, Universal shift register	BB	T_{X1}/pp 253-257,T_{X1}/pp 261-267, Ex1/pp 293-307, Tx2/pp 316, Tx2/pp 666
35	L35	Shift register counters: Ring counter, Johnson counter	BB	T_{X1}/pp 289-293, Tx2/pp 302-316, Ex1/pp 307-317

36	L36	Sequence generator	BB	T$_{X1}$/pp 221-233,T$_{X1}$/pp 293-298, Ex1/pp 317-325 Ex1/pp 649-681
UNIT V –SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS				
37	L37	General model, classification of synchronous sequential circuits	BB	TX1/pp 436-451, Tx2/pp 379, Tx3/ pp 583-608
38	L38	Analysis of synchronous sequential circuits	BB	TX1/pp 451-457,TX1/pp 474-479, Tx2/pp 379, EX1/pp 422-469
39	L39	Design of synchronous sequential circuits	BB/PPT	TX1/pp 440-442, TX1/pp 469-474, Tx2/pp 379, EX1/pp 469-475
40	L40	Use of algorithmic state machine	BB	TX1/pp 457-464, Tx2/pp 379, Tx2/pp 379
41	L41	Analysis and design of fundamental mode asynchronous sequential circuit	BB	TX1/pp 464-469, Rx1/pp495-506
42	L42	Analysis and design of pulse mode asynchronous sequential circuit	BB	TX1/pp 469-474, Tx2/pp 220-231, EX1/pp 471-474
43	L43	Incompletely specified state machines, Problems in asynchronous sequential circuit	BB	EX1/pp 475-480, TX1/pp 471-472, TX1/pp 369-384,
44	L44	Hazards, Types of hazards, Design of Hazard free switching circuits	BB/PPT	TX1/pp 469-474
45	L45	Hardware Description Language: Introduction to VHDL, VHDL model for combinational and sequential circuits	BB/PPT	TX1/pp 120-129,174-189,293-298

UNIT - I   MINIMIZATION TECHNIQUES AND LOGIC GATES
PART-A

1.1 Define Binary Logic.

Binary logic consists of binary variables and logic operations. The variables are designated by the alphabets such as A,B,C,x,y,z,etc., with each variable having only two distinct values: 1 and 0. There are three basic logic operations: AND, OR and NOT.

1.2 Define the following terms: Boolean variable, complement, literal. (Remembering) (CO1)

    a. Variable: The symbol which represents an arbitrary element of Boolean algebra is known as variable. Any single variable or a function of several variables can have either a 0 or 1.

    Example: Y = A + BC, variables A, B, and C can have either a 1 or 0 value, and function Y also can have either a 1 or 0 value.

    b. Complement: A complement of a variable is represented by a "bar" over the letter. For example, the complement of variable A is represented by A or A'.

    c. Literal: Each occurrence of a variable in Boolean function either in a complemented or un-complemented form is called a literal.

1.3 List the fundamental postulates of Boolean algebra. (Remembering) (CO1)

    The postulates of a mathematical system form the basic assumption from which it is possible to deduce the theorems, laws and properties of the system.

a. **Closure:** Closure with respect to the operator + : When two binary elements are operated by operator + the result is a unique binary element.

      Closure: Closure with respect to the operator . (dot) : When two binary elements are operated by operator . (dot), the result is a unique binary element.

b. An identity element with respect to +, designated by 0: A + 0 = 0 + A = A

  An identity element with respect to . (dot), designated by 1: A . 1 = 1 . A = A

c. Commutative with respect to + : A + B = B + A

  Commutative with respect to . (dot) : A . B = B . A

d. Distributive property of . (dot) over + : A . (B + C) = (A . B) + (A . C)
   Distributive property of + over . (dot) : A + (B . C) = (A + B) . (A + C)
e. Associative property of + : A + (B + C) = (A + B) + C
   Associative property of . : A . (B . C) = (A . B) . C
f. For every binary element, there exists complement element. For example, if A is an element, we
   have A′ is a complement of A i.e., if A = 0, then A′ = 1 and vice versa.
g. There exist at least two elements, say A and B in the set of binary elements such that A not
   equals B.

1.4 What are the applications of Boolean algebra? (MAY/JUNE 2010) (Remembering) (CO1)
     It is a convenient and systematic method of expressing and analyzing the operation of digital circuits and systems. Boolean algebra uses binary arithmetic variables which have two distinct symbols 0 and 1.

1.5 State the commutative property of Boolean algebra. (Remembering) (CO1)
     The commutative property states that the order in which the variables are OR- ed makes no difference. The commutative property is: A+B=B+A

1.6 State the distributive property of Boolean algebra. (Remembering) (CO1)
     The distributive property states that AND- ing several variables and OR- ing the result with a single variable is equivalent to OR -ing the single variable with each of the the several variables and then AND -ing the sums. The distributive property is: A+BC = (A+B) (A+C).

1.7 State the associative property of Boolean algebra. (Dec 2013/Jan 2014) (Remembering) (CO1)
     The associative property of Boolean algebra states that the OR(AND)- ing of several variables results in the same regardless of the grouping of the variables. The associative property is stated as follows:A+ (B+C) = (A+B) +C   A . (B . C) = (A . B) . C

1.8 State the absorption law of Boolean algebra. (Remembering) (CO1)
The absorption law of Boolean algebra is given by X+XY=X, X(X+Y) =X.

1.9 What are the three laws of Boolean algebra? (Remembering) (CO1)
     i) Commutative Law: A+B=B+A ii) Associative Law:A+(B+C)= (A+B)+C
iii) Distributive Law: A(B+C)=AB+AC

1.10 Write down the basic rules of Boolean algebra. (MAY/JUNE 2010,NOV/DEC 2010)
(Remembering) (CO1)
     a) A+0=A b) A+1=A c) A.0=0 d) A .1=A e) A+A=A f) A+A′=1 g) AA=A h) AA′=0 i) A=A   j)
     A+AB=A k) A+A′B=A+B l) (A+B)(A+C)=A+BC.

1.11 Label the two basic types of Boolean expressions. (Nov/Dec 2011) (Remembering) (CO1)
     i) Sum of Products (SOP) ii) Product of Sum (POS)

1.12 State De Morgan's theorem. (Dec 2009,May/June 2010,May/June 2013) (Remembering) (CO1)
     De Morgan suggested two theorems that form important part of Boolean algebra.
They are,
     1) The complement of a product is equal to the sum of the complements.(AB)' = A' + B'.
     2) The complement of a sum term is equal to the product of the complements.(A + B)' = A'B'.

1.13 List any two advantages of De-Morgan′s Theorem. (Remembering) (CO1)
   (i) It is used in simplifying the Boolean expressions. (ii) It allows the implementation of same Boolean expression using different logic gates (NAND or NOR).

1.14 Define duality property.(May/June 2012) (Remembering) (CO1)
     Duality property states that every algebraic expression deducible from the postulates of Boolean algebra remains valid if the operators and identity elements are interchanged. If the dual of an algebraic expression is desired, we simply interchange OR and AND operators and replace 1's by 0's and 0's by 1's.

1.15 Define Boolean expression. (Remembering) (CO1)
     Boolean expressions are constructed by connecting the Boolean constants and variables with the Boolean operations. These Boolean expressions are also known as Boolean formulas. Boolean expressions are used to describe switching function or Boolean functions. For example, if the Boolean expression (A + B′) C is used to describe the function f, then Boolean function is written as

f (A, B, C) = (A + B′) C or f = (A + B′) C.

1.16 What is sum of product form? (Remembering) (CO1)

A product term is any group of literals that are ANDed together. For example, ABC, XY, and so on. A sum term is any group of literals that are ORed together such as A + B + C, X + Y and so on. A sum of products (SOP) is a group of product terms ORed together.

For example (A, B, C) = AB + AB′C′

1.17 What is product of sum form? (Remembering) (CO1)

A product of sums (POS) is any groups of sum terms ANDed together.

For example, f (A, B, C) = (A + B + C) . (B′ + C)

1.18 What are standard SOP and POS forms? (Remembering) (CO1)

If each term in sum of product (SOP) form contains all the literals then the SOP form is known as standard or canonical SOP form. If each term in Product of sum (POS) form contains all the literals then the POS form is known as standard or canonical POS form.

1.19 Convert the given expression in standard SOP form: f (A, B, C) = AC + AB + BC. (Understanding) (CO1)

Step 1: Finding missing literal in each product term

AC = Literal B is missing, AB = Literal C is missing, BC = Literal A is missing

Step 2: AND product term with (missing literal + its complement)

f (A, B, C) = AC (B + B′) + AB (C + C′) + BC (A + A′)

Step 3: Expand the terms and reorder literals

f (A, B, C) = ABC + AB′C + ABC + ABC′ + ABC + A′BC

Step 4: Omit repeated product terms (allowing only one time)

f (A, B, C) = ABC + AB′C + ABC + ABC′ + ABC + A′BC Since A + A = A

f (A, B, C) = ABC + AB′C + ABC′ + A′BC

1.20 Write short note on tri-state gates. (Understanding) (CO1)

In addition to the normal output state (logic 0 and logic1), these gates can generate a third output state called High impedance (denoted by Z). These gates are having additional control input (CNTL), which when enabled produces normal output states; otherwise it makes the output into high impedance (open circuit) state. Under this condition the output becomes independent of input. The example for tri-state gate includes tri-state buffers and tri-state inverters.

1.21 What are the methods adopted to reduce Boolean function? (Remembering) (CO2)

i) Karnaug map ii) Tabular method or Quine Mc-Cluskey method iii) Variable entered map technique

1.22 Find the minterms of the logical expression Y = A'B'C' + A'B'C + A'BC + ABC.(Evaluating) (CO2)

Y = A'B'C' + A'B'C + A'BC + ABC' =m0 + m1 +m3 +m6 =_m(0, 1, 3, 6)

1.23 Write the maxterms corresponding to the logical expression Y = (A + B + C')(A + B' + C')

(A' + B' + C). (Understanding) (CO2)

Y = (A + B + C')(A + B' + C')(A' + B' + C) = (A + B + C')(A + B' + C')(A' + B' + C)

=M1.M3.M6 =_ M(1,3,6)

1.24 What is a karnaugh map? (Remembering) (CO2)

A karnaugh map or k map is a pictorial form of truth table, in which the map diagram is made up of squares, with each squares representing one minterm of the function.

1.25 State the limitations of Karnaugh map. (Remembering) (CO2)

i) Generally it is limited to six variable map (i.e) more then six variable involving expression are not reduced.ii) The map method is restricted in its capability since they are useful for simplifying only Boolean expression represented in standard.

1.26 What are called don't care conditions? (Remembering) (MAY/JUNE 2013) (CO2)

In some logic circuits certain input conditions never occur, therefore the corresponding output never appears. In such cases the output level is not defined, it can be either high or low. These output levels are indicated by 'X' or d' in the truth tables and are called don't care conditions or incompletely specified functions.

1.27 Explain or list out the advantages and disadvantages of K-map method?(DEC2009) (Remembering) (CO2)

The advantages of the K-map method are i. It is a fast method for simplifying expression up to four variables. ii. It gives a visual method of logic simplification. iii. Prime implicants and essential prime implicants are identified fast. iv. Suitable for both SOP and POS forms of reduction. v. It is more suitable for class room teachings on logic simplification.The disadvantages of the K-map method are i. It is not suitable for computer reduction. ii. K-maps are not suitable when the number of variables involved exceed four. iii. Care must be taken to fill in every cell with the relevant entry, such as a 0, 1 (or) don't care terms.

1.28 What is tabulation method? (Remembering) (CO2)

A method involving an exhaustive tabular search method for the minimum expression to solve a Boolean equation is called as a tabulation method.

1.29 List out the advantages and disadvantages of Quine-Mc Cluskey method? (Remembering) (CO2)

The advantages are, a. This is suitable when the number of variables exceed four. b. Digital computers can be used to obtain the solution fast. c. Essential prime implicants, which are not evident in K-map, can be clearly seen in the final results. The disadvantages are, a. Lengthy procedure than K-map. b. Requires several grouping and steps as compared to K-map. c. It is much slower. d. No visual identification of reduction process. e. The Quine Mc-Cluskey method is essentially a computer reduction method.

1.30 What is a prime implicant? (Remembering) (CO2)

A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map.

1.31 What is an essential implicant? (Remembering) (CO2)

If a minterm is covered by only one prime implicant, the prime implicant is said to be essential.

1.32 Simplify the given Boolean expression F=x' + xy + xz' + xy'z'.(NOV/ DEC 2012)(Analyzing) (CO2)

F=x' + xy + xz' + xy'z'
= x'+y + xz'(1+y')   A+A'B=A+B
= x'+y+xz'   1+A=1
= x'+z'+y   A+A'B=A+B

1.33 What is a Logic gate? (Remembering) (CO2)

Logic gates are the basic elements that make up a digital system. The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logical function

1.34 What are the basic digital logic gates? (Remembering) (CO2)

The three basic logic gates are AND gate OR gate NOT gate

**1.35 Which gates are called as the universal gates? What are its advantages?** (Remembering) (CO2)

The NAND and NOR gates are called as the universal gates. These gates are used to perform any type of logic application.

1.36 Determine the Implementation of the given function using NAND gates F(x,y,z)= Σm(0,6). (NOV/ DEC 2012) (Evaluating) (CO2)
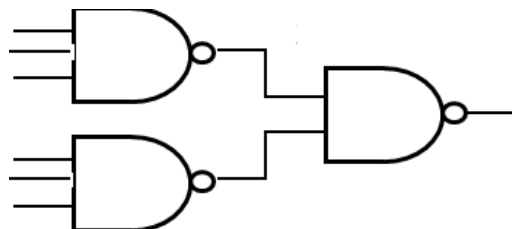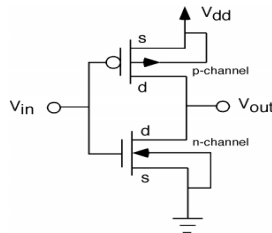

1.37 What is meant by tri-state gates? (MAY/JUNE 2012) (Remembering) (CO2)

It exhibits 3 possible output state conditions. There are 0, 1 & high impedance (z) state.
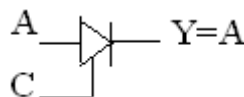
C = Control input

1.38 Show the CMOS inverter circuit. (NOV/DEC 2011)(Understanding) (CO2)

1.39 Find the complement of F=wx+yz then show that FF′=0. (APRIL/MAY 2011) (Evaluating) (CO1)

$$F=wx+yz$$
$$F'=(wx+yz)'$$

Therefore $\quad F.F'= (wx+yz).(wx+yz)'$

$$=0 \quad A.A'=0$$

1.40 Convert (AB+C)(B+C′D) into sum of products form. (APRIL/MAY 2011) (Understanding)(CO2)

Let $\quad Y=(AB+C)(B+C'D)$
$$=AB.B+ABC'D+BC+BC'D$$
$$=AB+ABC'D+BC+BC'D$$

1.41 Show that the positive logic NAND gate is negative logic NOR gate. (APRIL/MAY 2011) (Understanding) (CO1)

2-Input NAND Gate

Input		Output
A	B	
L	L	H
L	H	H
H	L	H
H	H	L

2-Input NOR Gate

Input		Output
A	B	
L	L	H
L	H	L
H	L	L
H	H	L

For a Positive logic put H=1 and L=0
For a Negative logic put H=0 and L=1
Then the truth table of the two gates will be:
2-Input Positive Logic NAND Gate

Input		Output
A	B	
0	0	1
0	1	1
1	0	1
1	1	0

2-Input Negative Logic NOR Gate

Input		Output
A	B	
0	0	1

0	1	1
1	0	1
1	1	0

1.42 Simplify F=Σ(1,4,5,6,7,13) using K-map. (NOV/DEC 2010,APRIL/MAY 2011)(Analyzing) (CO2)

$F=A'BC'+A'C'D+BC'D+A'BD$

1.43 Outline the CMOS logic circuit for NOR gate. (APRIL/MAY 2011)(Understanding) (CO2)
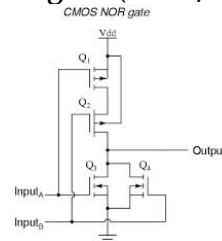
1.44 Prove that A+A'B = A+B.(NOV/DEC 2010) (Evaluating)(CO2)

$A+A'B = A+AB+A'B$ $A+AB=A$
         $= A+B.(A+A')$
        $=A+B.1$ $A+A'=1$
        $=A+B$

1.45 Show a tri-state inverter and draw its truth table. (NOV/DEC 2010) (Understanding)(CO2)
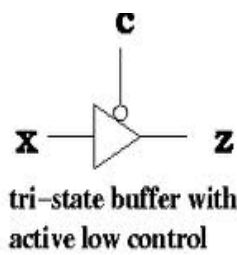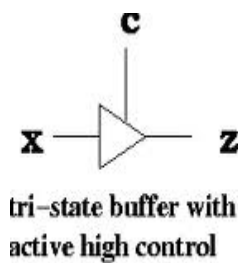
E	A	Z
0	0	High impedance
0	1	High impedance
1	0	0
1	1	1

1.46 Simplify the expression AB + (AC)' + AB'C(AB + C). (MAY/JUNE 2010)(Analyzing) (CO2)
AB + (AC)' + AB'C(AB + C) = AB + (AC)' + AAB'BC + AB'CC
        = AB + (AC)' + AB'CC [A.A' = 0]
        = AB + (AC)' + AB'C [A.A = 1]
        = AB + A' + C' =AB'C [(AB)' = A' + B']
        = A' + B + C' + AB'C [A + AB' = A + B]
        = A' + B'C + B + C' [A + A'B = A + B]
        = A' + B + C' +B'C
        = A' + B + C' +B'
        = A' + C' + 1
        = 1 [A + 1 =1]

1.47 Determine canonical SOP form of the function Y=AB+ACD. (MAY/JUNE 2010) (Evaluating) (CO2)
        Y=AB+ACD
         =AB(C+C')(D+D')+ACD(B+B')

=ABCD+ABCD′+ABC′D+ABC′D′+ABCD+AB′CD

= ABCD+ABCD′+ABC′D+ABC′D′+AB′CD

1.48 Find the complement of the functions F1 = x'yz' + x'y'z and F2 = x(y'z' + yz). (MAY/JUNE 2010) (Evaluating) (CO1)

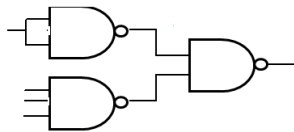F1' = (x'yz' + x'y'z)' = (x'yz')'(x'y'z)' = (x + y' + z)(x + y +z')

F2' = [x(y'z' + yz)]' = x' + (y'z' + yz)' = x' + (y'z')'(yz)' = x' + (y + z)(y' + z')

1.49 Write the truth table of 3-input OR gate. (MAY/JUNE 2010) (CO2) (Understanding)

TRUTH TABLE

INPUTS			OUTPUT
W	X	Y	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

1.50 Translate the expression , Y=A+BCD′ into realization using NAND gates. (MAY/JUNE 2010) (Understanding) (CO2)

1.51What is meant by minterm and maxterm? (DEC 2009) (Remembering) (CO2)

Each individual term in SOP is called minterm and in POS is called maxterm.

1.52 State advantages and disadvantages of TTL .

Adv: 1.Easily compatible with other ICs 2.Low output impedance

Disadv: 1.Wired output capability is possible only with tristate and open collector types

2.Special circuits in Circuit layout and system design are required.

1.53 What are the types of TTL logic?

1. Open collector output 2. Totem-Pole Output 3. Tri-state output.

1.54 What is depletion mode operation MOS?

If the channel is initially doped lightly with p-type impurity a conducting channel exists at zero gate voltage and the device is said to operate in depletion mode.

1.55 What is enhancement mode operation of MOS?

If the region beneath the gate is left initially uncharged the gate field must induce a channel before current can flow. Thus the gate voltage enhances the channel current and such a device is said to operate in the enhancement mode.

1.56 Mention the characteristics of MOS transistor?

1. The n- channel MOS conducts when its gate- to- source voltage is positive. 2. The   p-channel MOS conducts when its gate- to- source voltage is negative. 3. Either type of device is turned off if its gate- to- source voltage is zero.

1.57 How schottky transistors are formed and state its use?

A schottky diode is formed by the combination of metal and semiconductor. The presence of schottky diode between the base and the collector prevents the transistor from going into saturation. The resulting transistor is called as schottky transistor.

The use of schottky transistor in TTL decreases the propagation delay without a sacrifice of power dissipation.

1.58 List the different versions of TTL

1.TTL (Std.TTL) 2.LTTL (Low Power TTL) 3.HTTL (High Speed TTL) 4.STTL (Schottky TTL) 5.LSTTL (Low power Schottky TTL)

1.59 Why totem pole outputs cannot be connected together ?

Totem pole outputs cannot be connected together because such a connection might produce excessive current and may result in damage to the devices.

1.60 What happens to output when a tristate circuit is selected for high impedance ?

Output is disconnected from rest of the circuits by internal circuitry.

1.61 What does LS in 74LS00 indicate?(DEC 2009) (Remembering) (CO1)

LS represents Low Power Schottky TTL Series.

1.62 Define Boolean algebra & Boolean Expression.

A system of algebra that operates on Boolean variables. The binary nature of Boolean algebra makes it useful for analysis,simplification and design of logic circuits.

1.63 Define Pair, Quad, and Octet.

i). Pair: A group of two adjacent cells in a karnaugh map. A pair cancels one variable in a K-Map simplification.

ii). Quad: A group of four adjacent cells in a karnaugh map. A quad cancels two variable in a K-Map simplification.

iii). Octet: A group of eight adjacent cells in a karnaugh map. A pair cancels three variable in a K-Map simplification.

PART-B

1. (a) Reduce the following Boolean expression A′B′C′+A′BC′+A′BC.(Dec 2013/Jan 2014)**(Evaluating)** (CO1)

   (b) Simplify the following expression Y=(A+B)(A+C′)(B′+C′). (Dec 2013/Jan 2014)(Analyzing) (CO1)

2. (a) Which gates are called as the universal gates? What are its advantages? (Dec 2013/Jan 2014) (Remembering) (CO1)

   (b) Discuss CMOS NAND gate operation.(Understanding) (CO1)

3. Minimize the given switching function using Quine-Mcclusky method.

 $f(x_1,x_2,x_3,x_4)=\Sigma(0,5,7,8,9,10,11,14,15)$ (Dec 2009,April/May 2011,Nov/Dec 2012,May/June 2013) (Evaluating) (CO1)

 4. Simplify the given Boolean function into (i) Sum of products form (ii) Product of sum form and implement it using basic gates. $F(A,B,C,D)=\Sigma(0,1,2,5,8,9,10)$ (May/June 2010,May/June 2013) (Analyzing) (CO1)

5.Find the MSP representation for $F(A,B,C,D,E)=\Sigma m(1,4,6,10,20,22,24,26)+\Sigma d(0,11,16,27)$ using K-map method. Draw the circuit of the minimal expression using only NAND gates. (Dec 2009,May/June 2012) (Evaluating) (CO1)

6. Explain in detail about the CMOS logic based gate circuits with its characteristics. (May/June 2012) (Understanding) (CO1)

7. Simplify the following Boolean function by using Quine-Mcclusky method and also verify the same using by using Karnaugh map.

$F(A,B,C,D)=\Sigma(0,2,3,6,7,8,10,12,13)$ (May/June 2010,Nov/Dec 2010,Nov/Dec 2011) (Evaluating) (CO1)

8. Draw symbol, truth table and the equation of the three basic gates and two universal gates and realize all the five gates using either of the universal gates. (Nov/Dec 2011) (Understanding)(CO1)

9. Implement F=(A′B+AB′)(C+D′) using NOR gates. (Nov/Dec 2010) (Evaluating) (CO1)

10.Simplify the expression Π (0,1,4,5,6,8,9,12,13,14) using K-map method. (Dec 2009,May/June 2010) (Evaluating)(CO1)

UNIT - II   COMBINATIONAL CIRCUITS

PART-A

2.1 Define combinational logic. Give examples.(DEC 2013/JAN 2014) (Remembering) (CO2)

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called combinational logic.

2.2Explain the design procedure for combinational circuits. (Understanding) (CO2)

1. The problem definition

2. Determine the number of available input variables & required output variables.

3. Assigning letter symbols to input and output variables
4. Obtain simplified Boolean expression for each output.
5. Obtain the logic diagram.

2.3 Define Half adder and full adder. (DEC 2009,DEC 2013/JAN 2014) (Remembering) (CO2)
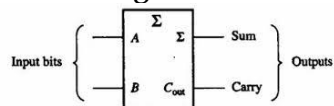
The logic circuit that performs the addition of two bits is a half adder. The circuit that performs the addition of three bits is a full adder.

**2.4 What is the limitation of half adder?** (Remembering) (CO2)

In multi-digit addition we have to add two bits along with the carry of the previous digit addition. Effectively such addition requires addition of three bits. This is not possible with half-adder. Hence half-adders are seldom used in practice

2.5 Represent a half adder in block diagram form and also its logic implementation.(NOV/DEC 2010) (Understanding) (CO2)

Block Diagram

Logic Diagram
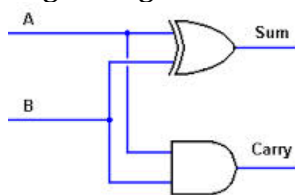
2.6 Implement a full adder using two half adder. (APRIL/MAY 2011) (Evaluating) (CO2)
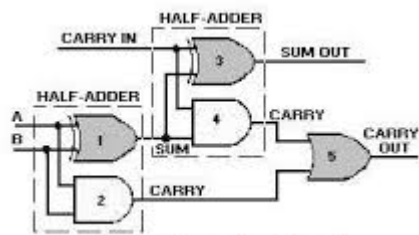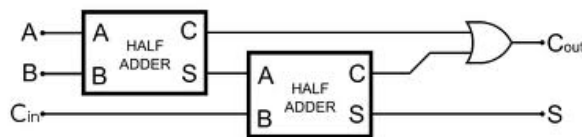
2.7 What is half-subtractor? (DEC2008) (Remembering) (CO2)

The combinational circuit that performs the subtraction of two bits are called a half-subtractor.

2.8 What is a full-subtractor? (Remembering) (CO2)

The combinational circuit that performs the subtraction of three bits is called a half-subtractor.

2.9 Design a Half-subtractor using basic gates. (MAY/JUNE 2013) (Creating) (CO2)
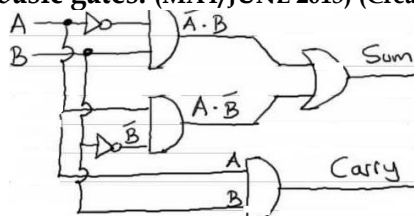
2.10 Draw the logic diagram of a serial adder. (NOV/ DEC 2012)(Understanding) (CO2)
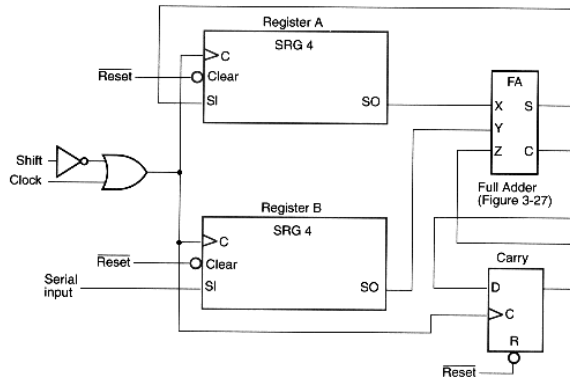
2.11 What is a parallel Adder? (Remembering) (CO2)

A single full-adder is capable of adding two one-bit numbers and an input carry. In order to add binary numbers with more than one bit, additional full-adders must be employed. A n-bit parallel can be constructed using number of full adder circuits connected in parallel.
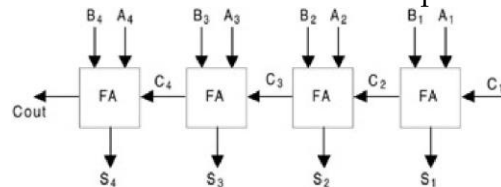

Figure: Four bit Parallel Adder

2.12 What is the drawback in binary parallel adder? How it can be rectified? (Remembering) (CO2)

The parallel adder is ripple carry adder in which the carry output of each full-adder stage is connected to the carry input of the next higher-order stage. Therefore, the sum and carry outputs of any stage cannot be produced until the input carry occurs; this leads to time delay in the addition process. The delay is known as carry propagation delay.

One method of speeding up the process by eliminating inter stage carry delay is called look-ahead carry addition. This method utilizes logic gates to look at the lower order bits of the augend and addend to see if a higher-order carry is to be generated.

2.13 Write the principle of carry look ahead logic. (APRIL/MAY 2011) (Remembering) (CO2)

For each bit in a binary sequence to be added, the Carry Look Ahead Logic will determine whether that bit pair will generate a carry or propagate a carry. This allows the circuit to   "pre-process" the two numbers being added to determine the carry ahead of time. Then, when the actual addition is performed, there is no delay from waiting for the ripple carry effect (or time it takes for the carry from the first Full Adder to be passed down to the last Full Adder)

2.14 Compare binary serial adder and parallel adder.(Understanding) (CO2)

S. No	Serial Adder	Parallel Adder
1	Serial adder uses shift registers	Parallel adder uses registers with parallel load
2	The serial adder requires only one full -adder circuit	The number of full adder circuits in the parallel adder equal to the number of bits in the binary numbers
3	The serial adder is a sequential circuit	Excluding the registers, the parallel adder is a purely combinational circuit
4	Time required for addition depends on number of bits.	Time required for addition does not depend on number of bits.
5	It is slower	It is faster

2.15 Define BCD adder and its function. (MAY/JUNE 2010) (Remembering) (CO2)

A BCD adder is a circuit that adds two BCD digits and produces a sum digit which is also in BCD. When two BCD numbers are added and if the sum is less than or equal to 9 the result obtained is correct BCD result. If the sum is greater than 9, the result is incorrect BCD and a correction factor of 6 is added to get correct BCD result.

2.16 What is code converter? (Remembering) (CO2)

It is a circuit that makes the two systems compatible even though each uses a different binary code. It is a device that converts binary signals from a source code to its output code. One example is a BCD to Excess-3 code converter

2.17 What is the need for code converters? (Remembering) (CO2)

There is a wide variety of binary codes used in digital systems. Some of these codes are binary-coded decimal (BCD), excess-3, Gray code and so on. Many times it is required to convert one code to another.

2.18 Give the practical uses of code-converter circuits. (MAY/JUNE 2012) (Remembering) (CO2)

Code conversion is a widely used process used in digital systems for reasons such as enhancing security of data, reducing the complexity of arithmetic operations and thereby reducing the hardware required, dropping the level of switching activity leading to more speed of operation and power saving etc.

2.19 What do you mean by comparator? (Remembering) (CO2)

It is a special combinational circuit designed primarily to compare the relative magnitudes of two binary numbers. An n-bit comparator receives two n-bit binary A and B, and the outputs are: A > B, A < B, and A = B. As per the magnitudes of the two numbers, one of the three outputs will be high.

2.20 What are parity generators and parity checkers? (Remembering) (CO2)

A circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker. It must be noted here that a parity bit is used for the purpose of detecting errors during transmission of binary information. A parity bit is an extra bit included with a binary message to make the number of 1s either odd or even.

2.21 Design a three bit even parity generator. (NOV/ DEC 2012) (Creating) (CO2)

D1	D2	D3	Even-Parity
0	0	0	True
0	0	1	False
0	1	0	False
0	1	1	True
1	0	0	False
1	0	1	True
1	1	0	True
1	1	1	False
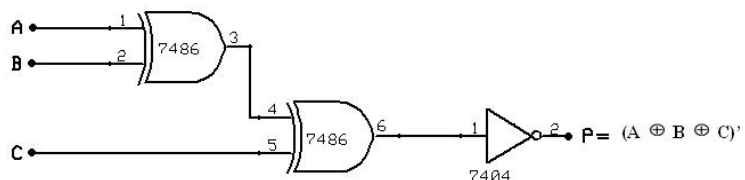
2.22 Why parity generator necessary? (DEC 2008) (Remembering) (CO2)

Parity generator is essential to generate parity bit in the transmitter.

**2.23 Why parity checker is needed?(DEC 2008) (Remembering) (CO2)**

Parity checker is required at the receiver side to check whether the expected parity is equal to the calculated parity or not. If they are not equal then it is found that the received data has error.

2.24 Give the comparison between combinational and sequential circuits. (NOV/ DEC 2011) (Understanding) (CO2)

S. No	Combinational circuits	Sequential circuits
1	In combinational circuits, the output variables are at all times dependent on the combination of input variables	In sequential circuits, the output variables depend not only on the present input variables but they also depend upon the past history of input variables
2	Memory unit is not required in combinational circuits	Memory unit is required to store the past history of input variables in sequential circuits

3	Combinational circuits are faster in speed because the delay between input and output is due to propagation delay of gates.	Sequential circuits are slower than the combinational circuits
4	Combinational circuits are easy to design	Sequential circuits are comparatively harder to design
5	Parallel adder is combinational circuit	Serial adder is a sequential circuit

2.25 Why multiplexer is called as Data Selector? (MAY 2010) (MAY 2013) (Remembering)(CO2)
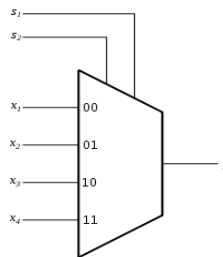
Multiplexer is called as Data Selector since it selects one of the many inputs and steers the information to the output.

2.26 What is Demultiplexer? (DEC 2009) (Remembering) (CO2)

A Demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2n possible output lines.

2.27 Give the other name for Multiplexer and Demultiplexer. (MAY/JUNE 2010) (Remembering) (CO2)

Multiplexer is otherwise called as Data selector. Demultiplexer is otherwise called as Data distributor.

2.28 Give the applications of Demultiplexer. (Remembering) (CO2)

i) It finds its application in Data transmission system with error detection. ii) One simple application is binary to Decimal decoder.

2.29 What is encoder? (Remembering) (CO2)

A encoder is a combinational circuit that converts binary information from 2^n Input lines to a maximum of 'n' unique output lines.

2.30 What is decoder? MAY/JUNE 2010(Remembering) (CO2)

A decoder is a combinational circuit that converts binary information from 'n' input lines to a maximum of 2^n unique output lines.

2.31 What is priority encoder? (Dec 2009) (Remembering) (CO2)

A priority encoder is an encoder that includes the priority function. The operation of the priority encoder is such that if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

2.32 How does encoder differs from decoder.(May 2010) (Remembering) (CO2)

An encoder is a digital circuit that performs the inverse operation of decoder. An encoder is a combinational logic circuit that converts an active input signal in to a coded output signal.

2.33 List out the applications of decoder? (DEC 2010) (Remembering) (CO2)

The applications of decoder are a. Decoders are used in counter system. b. They are used in analog to digital converter. c. Decoder outputs can be used to drive a display system.

2.34 Can a decoder function as a Demultiplexer?(MAY2011) (Evaluating) (CO2)

Yes. A decoder with enable can function as a Demultiplexer if the enable line E is taken as a data input line A and B are taken as selection lines.

PART-B

1.Explain the design procedure for combinational circuits. (Dec 2013/Jan 2014)(Evaluating) (CO2)

2.Explain the working of full adder.(DEC 2009) (Evaluating) (CO2)

3.Design a logic circuit to convert the BCD code to Excess-3 code. (DEC 2009,Nov/Dec 2010,Nov/Dec 2012,Dec 2013/Jan 2014) (Creating) (CO2)

4.Explain the operation of magnitude comparator. (Dec 2013/Jan 2014) (Evaluating) (CO2)

5.Design a BCD adder and explain its working with necessary circuit diagram.
(Nov/Dec 2011May/June 2013) (Creating) (CO2)

6.Design a 4-bit magnitude comparator. (May/June 2012,May/June 2013) (Creating) (CO2)

7.Design a 4-bit parallel adder/subtractor and draw the logic diagram. (Nov/Dec 2011,Nov/Dec 2012) (Creating) (CO2)

8.Design a 4-bit multiplier and binary divider circuit with detail operation. (May/June 2012) (Creating) (CO2)

9.Design a BCD to Gray code converter. Use don't care. (Nov/Dec 2011) (Creating) (CO2)

10.Design a 4-bit binary to gray code converter. (Creating) (CO3)

11.(a) Design a four bit parity checker and generator. (Creating) (CO2)

(b) Design a single bit magnitude comparator.(April/May 2011) (Creating) (CO2)

12.Design a combinational circuit that converts a four bit gray code to four bit binary number. (April/May 2011) (Creating) (CO2)

(a) Design a combinational circuit that performs the arithmetic sum of three input bits and produces a sum and carry output. (Creating) (CO2)

(b) IC 7485 4-bit magnitude comparator has A=1011 and B=1001 (a) Determine the outputs (b) Show how to connect <, =, and > inputs if this is to be the least significant stage. (May/June 2010) (Evaluating) (CO2)

13. Implement the following function using 4X1 and 8:1 MUX multiplexer F(A,B,C)=∑(1,3,5,6) (Dec 2010) (May2010) (May2011) (Dec 2013) (Evaluating) (CO2)

14. Construct a 5X32 decoder with four 3X5 decoders and a 2X4 decoder. Use block diagrams. (Dec 2013) (Creating) (CO2)

UNIT - III   MEMORY AND PROGRAMMABLE LOGIC DEVICES

PART-A

3.1 Define memory Expansion. (Remembering)(CO3)

Memory IC's can be connected together to expand the number of memory words or the number of bits per word.

3.2 Explain FPGA. (Dec2009) (Understanding) (CO3)

Field Programmable gate Arrays(FPGA) is a flexible architecture programmable logic device. It's a single Very Large Scale Integrated(VLSI) circuit constructed on a single piece of silicon.

3.3 Classify the memories. (DEC 2012) (Remembering) (CO3)

1. Registers, main memory and secondary memory. 2. Sequential access memory and random access memory 3. Static and dynamic memory 4. Volatile and non volatile memory.
5. Magnetic and semiconductor memory.

3.4 What is RAM? (May2011) (Remembering) (CO3)

Random-access memory (RAM /ræm/) is a form of computer data storage. A random-access memory device allows data items to be read and written in roughly the same amount of time regardless of the order in which data items are accessed.[1] In contrast, with other direct-access data storage media such as hard disks, CD-RWs, DVD-RWs and the older drum memory, the time required to read and write data items varies significantly depending on their physical locations on the recording medium, due to mechanical limitations such as media rotation speeds and arm movement delays.

3.5 What is ROM? (MAY2012) (Remembering) (CO3)

It is a device that includes both the decoder and the OR gates with in a single IC package. ROM does not full decoding of the variables and does generate all the minterms.

3.6 Differentiate ROM & PLD's (MAY2012) (Understanding)(CO3)

ROM (Read Only Memory)	PLD's (Programmable Logic Devices)

It is a device that includes both the decoder and the OR gates with in a single IC package	It is a device that includes both AND and OR gates with in a single IC package
ROM does not full decoding of the variables and does generate all the minterms	PLD's does not provide full decoding of the variable and does not generate all the minterms

3.7 List the types of ROM. (NOV/DEC 2010) (MAY/JUNE 2010) (Remembering) (CO3)

i) Programmable ROM (PROM) ii) Erasable ROM (EPROM) iii) Electrically Erasable ROM (EEROM)

3.8 Compare PROM and EPROM.(MAY2007) (Understanding) (CO3)

PROM	EPROM
PROM once programmed, the fixed pattern is permanent and can not be altered.	EPROM can be restructured to the initial state, even though it has been programmed previously.

3. 9 List the different types of RAM. (DEC 2013) (Remembering) (CO3)

1.NMOS RAM 2.CMOS RAM 3. Schottky TTL RAM 4.ELL RAM

3.10 What are the advantages of RAM? (DEC 2009) (Remembering) (CO3)

a. Non-Destructive read out. b. Fast operating speed. c. Low power dissipation. d. Compatibility.

3.11 What are the terms that determine the size of a PAL? (Remembering)(CO3)

The size of a PAL is specified by the

a. Number of inputs b. Number of products terms c. Number of outputs

3.12 Draw the circuit of a MOSFET RAM cell. (NOV/DEC 2010) (Understanding) (CO3)
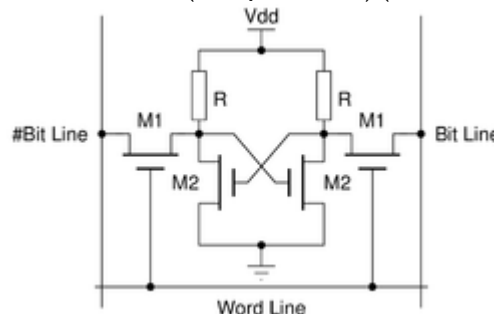
3.13 Draw the logic diagram of bipolar RAM cell. (DEC 2012) (Understanding) (CO3)
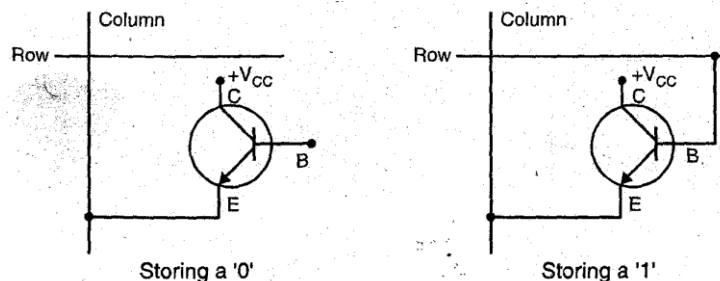
3.14 Differentiate volatile and non-volatile memory? (DEC2009) (DEC 2011) (Understanding) (CO3)

Volatile memory	Non-volatile memory
They are memory units which lose stored information when power is turned off. E.g. SRAM and DRAM	It retains stored information when power is turned off. E.g. Magnetic disc and ROM

3.15 Draw the basic configuration of PAL. (NOV/DEC 2010) (MAY 2013) (DEC 2013) (Understanding)(CO3)
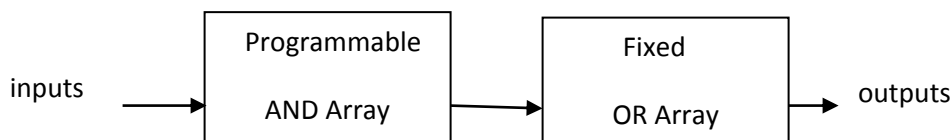
3.16 Draw the basic configuration of PLA. (Dec2009) (May 2013) (Understanding) (CO3)
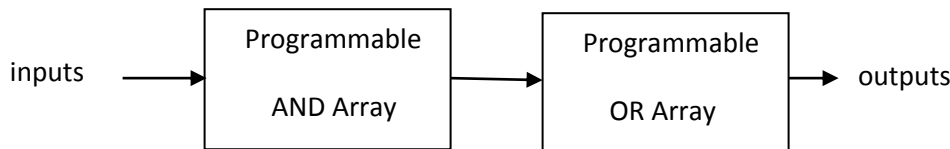
3.17 What are the different types of PLDs? (DEC 2011) (Remembering) (CO3)
a. Devices with fixed architecture. Eg. PLA, PAL. b. Devices with flexible architecture Eg. FPGA's.
3.18 List out the applications of PLAs.(MAY2010) (MAY 2013) (Remembering) (CO3)
        The PLAs are used to replace ROMs in many applications. They are used for implementing combinational logic functions and results in compact circuitry and high switching speed.
PART-B
1. With neat diagram explain the RAM organization? (Dec 2009) (Understanding) **(CO3)**
2. Define the following i) Static RAM ii) Dynamic RAM (Dec 2009) (Remembering) **(CO3)**
3. Show how a PAL is programmed for the following 3 variable logic function
X= A'BC'+AB'C'+A'B+AC (May 2010) (Understanding) **(CO3)**
4. Implement the following function using PLA. F1(x, y, z)= ∑m(1,2,4,6);F2(x, y, z) = ∑m(0,1,6,7); F3 (x, y, z) =∑m(2 ,6) (Dec 2009) (Evaluating) **(CO3)**
5. Explain the basic structure of a 256X4 static RAM with neat diagram. (Dec 2010) (Evaluating) **(CO3)**
6. Briefly explain about the various types of ROM and RAM cells. (May 2011) (Dec 2011) (May 2012) (Understanding) **(CO3)**
7. Implement the given function using PAL. A=∑m(0,2,6,7,8,9,12,13), B=Em(0,2,6,7,8,9,12,13,14), C=Em(1,3,4,6,10,12,13), D=Em(1,3,4,6,9,12,14)(Dec 2011) (May2013) (Evaluating) **(CO3)**
8. Implement binary to gray code converter using PROM devices. (Dec 2012) (May2013) (Evaluating) **(CO3)**
9. Explain about PLD and its merits. (Dec 2013) (Understanding) **(CO3)**

UNIT IV SEQUENTIAL CIRCUITS
PART-A
4.1 What is sequential circuit? (DEC 2009) (DEC 2013) (Remembering)(CO4)
        Sequential circuit is a broad category of digital circuit whose logic states depend on a specified time sequence. A sequential circuit consists of a combinational circuit to which memory elements are connected to form a feedback path.
4.2 What do you mean by triggering of flip-flop. (MAY 2010) (Remembering) (CO4)
        The state of a flip-flop is switched by a momentary change in the input signal. This momentary change is called a trigger and the transition it causes is said to trigger the flip-flop.
4.3 Mention the different types of triggering. (Remembering) (CO4)
 Ans: i. Level Triggering ii. Edge Triggering
4.4 Give the excitation table of a JK,SR, T& D flip-flop.(Nov/Dec 2010) (Understanding) (CO4)

PS	NS	FF I/P		FF I/P		FF I/P	FF I/P
Q(t)	Q(t+1)	J	K	S	R	T	D
0	0	0	X	0	X	0	0
0	1	1	X	1	0	1	1
1	0	X	1	0	1	1	0
1	1	X	0	X	0	0	1

4.5 What is an excitation table? (Remembering) (CO4)

During the design process we usually know the transition from present state to next state and wish to find the flip-flop input conditions that will cause the required transition. A table which lists the required inputs for a given chance of state is called an excitation table.

4.6 Give the characteristic equation of a SR, D, JK & T flip-flop. (Understanding) (CO4)

1) $Q(t+1)=S+R'Q$ 2)$Q(t+1)=D$ 3) $Q(t+1)=JQ'+K'Q$ 4)$Q(t+1)=TQ'+T'Q$

4.7 What is the difference between truth table and excitation table? (Remembering) (CO4)

i) An excitation table is a table that lists the required inputs for a given change of state. ii) A truth table is a table indicating the output of a logic circuit for various input states.

4.8 How many flip flops are required to built a binary counter that counts from 0 to 1023? (MAY 2013) (Remembering) (CO4)

Ans: 10

4.9 Give the applications of flip flop? (DEC 2009) (CO4)

Flip flops are used in many application such as Data storage, Data Transfer, Counters, Frequency divisions etc.

4.10 What is called latch? (Remembering) (CO4)

Latch is a simple memory element, which consists of a pair of logic gates with their inputs and outputs inter connected in a feedback arrangement, which permits a single bit to be stored.

4.11 What is a ring counter? (DEC 2012) (Remembering) (CO4)

A counter formed by circulating a 'bit' in a shift register whose serial output has been connected to its serial input.

4.12 What is up/down counter? (Remembering) (CO4)

A counter, which is capable of operating as an up counter or down counter, depending on a control lead.

4.13 What is Johnson counter? (Remembering) (CO4)

It is a ring counter in which the inverted output is fed into the input. It is also know as a twisted ring counter.

4.14 What are the uses of a counter? (Remembering) (CO4)

i) The digital clock ii) Auto parking control iii) Parallel to serial data conversion.

4.15 What is synchronous counter?(MAY2010) (Remembering) (CO4)

In a synchronous counter, the clock pulse is applied simultaneously to all flipflops. The output of the flip-flops change state at the same instant. The speed of operation is high compared to an asynchronous counter

4.16 Sketch the timing signals for a 4-bit ring counter. (MAY2011) (CO4)
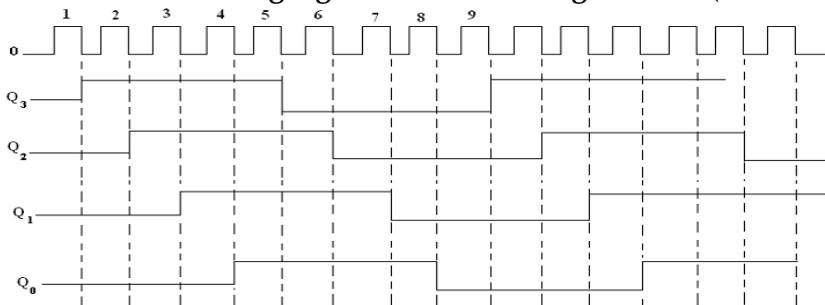
4.17 What is a shift register? And its types. (MAY 2010)(DEC 2013) (Remembering) (CO4)

In digital circuits, datas are needed to be moved into a register (shift in) or moved out of a register (shift out). A group of flip-flops having either or both of these facilities is called a shift register. Types are Serial in serial out shift register, serial in parallel out shift register, parallel in serial out shift register, parallel in parallel out shift register.

4.18 What is serial shifting? (Remembering) (CO4)

In a shift register, if the data is moved 1 bit at a time in a serial fashion, then the technique is called serial shifting.

4.19 What is parallel shifting? (Remembering) (CO4)

2. With neat diagram explain the different types of flip flops? (Dec 2009) (May 2012) (Dec 2013) **(CO4)**(Understanding)

3. Discuss in detail about JK flip flop with its truth table, state diagram and characteristics equation. (May 2010) **(CO4)** (Understanding)

4. Explain the working of master slave JK flip flop. State its merit. (May 2011) **(CO4)** (Understanding)

5. Draw the Johnson counter and explain the operation (Dec 2010) (Evaluating) **(CO4)**

6. Explain the working of BCD ripple counter/Decade with timing diagrams. (May 2010) (May 2012) (May2013) **(CO4)** (Evaluating)

7. Explain the operation of various types of shift register. (May 2010) (CO4) (Understanding)

8. Design a sequence detector that produces an output 1 whenever the non overlapping sequence 1011 is detected. (May 2010) (Dec 2012) (Dec 2013) **(CO4) (Creating)**

9. Design a 3 bit binary counter using T flip flop that has a repeated sequences of six states. 000-001-010-100-101-110. Give the state table, state diagram and logic diagram. (Dec 2010) (May2013) **(CO4)** (Creating)

10. Design a 4 bit universal shift register and explain its operation. (May 2011) (Dec 2012) **(CO4)**(Creating)

11. Design a MOD – 10 synchronous counter using J-K flip flops. Write the excitation table and state table. (Dec 2011) (Dec 2011) **(CO4)** (Creating)

12. Draw the logic diagram of a 4 bit up/down ripple counter using JK flip flop and explain its operation with timing diagram. (Dec 2011) (Dec 2012) **(CO4)**(Understanding)

UNIT V SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS

5.1. What is primitive flow table? **(DEC 2005), (DEC 2013) (Remembering)(CO5)**

A flow table is called Primitive flow table because it has only one stable state in each row.

5.2. What is flow table? **(NOV/DEC 2007) (Remembering))(CO5)**

During the design of synchronous sequential circuits, it is more convenient to name the states by letter symbols without making specific reference to their binary values. Such table is called Flow table.

5.3Define cycle and merging? **(NOV/DEC 2007) (Remembering))(CO5)**

When a circuit goes through a unique sequence of unstable states, it is said to have a cycle. The grouping of stable states from separate rows into one common row is called merging.

5.4 Define race condition. **(DEC2008) MAY/JUNE 2010, (NOV/DEC 2007), (DEC 2013) (Remembering)(CO5)**

A race condition is said to exist in a synchronous sequential circuit when two or more binary state variables change, the race is called non-critical race.

5.5 Differentiate fundamental mode and pulse mode asynchronous sequential circuits.(CO5)

In a fundamental mode circuit, all of the input signals are considered to be levels. Fundamental mode operation assumes that the input signals will be changed only when the circuit is in a stable state and that only one variable can change at a given time.

In pulse mode circuits, the inputs are pulses rather than levels. In this mode of operation the width of the input pulses is critical to the circuit operation. The input pulse must be long enough for the circuit to respond to the input but it must not be so long as to be present even after new state is reached. In such a situation the state of the circuit may make another transition. The minimum pulse width requirement is based on the propagation delay through the next state logic. The maximum pulse width is determined by the total propagation delay through the next state logic and the memory elements. Both fundamental and pulse mode asynchronous sequential circuits use unclocked S-R FLIP-FLOPs or latches.

5.6 Define the term stable state. **(JUNE 2012) (Remembering))(CO5)**

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bitable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

5.7 Differentiate Moore circuit and Mealy circuit? DEC2009,NOV/DEC 2010,AP/MAY 2005.(DEC2010),　　(Dec 2011) (CO5)

Moore circuit	Mealy circuit
a. It is output is a function of present state only.	a. It is output is a function of present state as well as the present input.
b. Input changes do not affect the output.	b. Input changes may affect the output of the circuit.
c. Moore circuit requires more number of states for implementing same function.	c. It requires less numbers of states for implementing same function.

5.8 . Define state assignment.(DEC2009) (Remembering) (CO5)

Assigning state variables (i.e., secondary variables) to the rows of merged primitive state table and obtain present state/Next state and output table. The output assigned to the unstable states vary accorcding to the design requirements.

5.9. Define pulse mode asynchronous sequential circuit. (DEC2009), JUNE 2012(Remembering) (CO5)

In pulse mode asynchronous sequential circuits, inputs and outputs are represented by pulses.

5.10 How can a race be avoided?(DEC2009), (NOV/DEC 2004) (Remembering) (CO5)

Races can be avoided by directing the circuit through intermediate unstable states with a unique state – variable change.

5.11 Write a note on dynamic hazards (MAY2010) MAY/JUNE 2010,May 2011(CO5)

When the output is supposed to change from 0 to 1 (or from 1 to 0), the circuit may go through three or more transients and produce more than one glitch. Such multiple glitch situations are known as dynamic hazard

5.12 How can the hazards in combinational circuit be removed? (Remembering) (CO5)

Hazards in the combinational circuits can be removed by covering any two min terms that may produce a hazard with a product term common to both. The removal of hazards requires the addition of redundant gates to the circuit.

5.13 Define race condition.(DEC2008) MAY/JUNE 2010, (NOV/DEC 2007) (Remembering) (CO5)

A race condition is said to exist in a synchronous sequential circuit when two or more binary state variables change, the race is called non-critical race.

5.14 Define critical & non-critical race with example.(DEC2007) NOV/DEC 2010, (NOV/DEC 2007) (Remembering) (CO5)

The final stable state that the circuit reaches does not depend on the order in which the state variables change, the race is called non-critical race. The final stable state that the circuit reaches depends on the order in which the state variables change, the race is called critical race.

5.15. Explain the design procedure for Fundamental mode asynchronous sequential circuits.(CO5)

a. From the verbal description of the problem, formulate precisely what the circuit has to do. b. Develop a primitive state table and specify the outputs that are associated with the stable state. c. Minimize the primitive state table by merge process. d. State Assignment: Assign state variable to the rows of merged primitive state table and obtain present state, next state and output table. e. Decide the memory element to be used and obtain excitation and output table obtain the simplified expression for excitation and output function. f. Draw the schematic circuit diagram.

5.16. Distinguish between synchronous sequential circuit and asynchronous sequential circuit. (DEC 2010). (Remembering)(CO5)

Synchronous Sequential Circuit: Output changes at discrete interval of time. It is a circuit based on an equal state time or a state time defined by external means such as clock. Examples of synchronous sequential circuit are Flip Flops, Synchronous Counter.

Asynchronous Sequential Circuit: Output can be changed at any instant of time by changing the input. It is a circuit whose state time depends solely upon the internal logic circuit delays. Example of asynchronous sequential circuit is Asynchronous Counter.

5.17 Define hazards. (MAY2008), (JUNE 2013) (Remembering) (CO5)

Hazards are unwanted switching transients that may appear at the output of a circuit because different paths exhibit different propagation delays.

5.18 What are the different modes of operation in asynchronous sequential circuits?DEC2012 (Remembering) (CO5)

   1. Fundamental Mode,2. Pulse Mode

5.19. What is meant by race around condition?(MAY2008) (Remembering)(CO5)

   In JK flip-flop output is fed back to the input, and therefore changes in the output results change in the input. Due to this in the positive half of the clock pulse if J and K are both high then output toggles continuously. This condition is known as race around condition.

PART-B

1.A sequential circuit has two JK flip flops A and B, two inputs x and y, and one output z. the flip flop input equations and circuit output equation are JA=BX+BX'Y' KA=B'XY' JB=A'X KB=A+XY' Z=AX'Y'+BX'Y' a) Tabulate the state table b) Derive the state equations for A and B (May 2011) **(CO5)**(Evaluating)

2. Define races and explain its types and hazards that occur in asynchronous circuits. Discuss a method used for race free assignment with example. **(DEC 2013),(DEC 2012), (JUNE 2012), (JUNE 2010),(DEC 2010)(DEC2013)(DEC2009) (CO5)**

3.Using suitable example, discuss about flow table. **(DEC 2013) (CO5)**

4.Design an asynchronous sequential circuit that has two internal states and one output. The excitation and output function describing the circuit are as follows.

X = x_1x_2 + x_1y_2+x_2y_1 Y = x_2 + $x_1y_1y_2$+ x_1y_1 Z = x_2 + y_1 **(DEC 2011). (CO5)**

5.Design a pulse mode circuit with three inputs x1, x2, x3 and one output z. The output z should change from 0 to 1, only for the input sequence x1-x2-x3.Also the output z should remain in 1 until x2 occurs. Use SR flip flop for the design. **MAY/JUNE 2009 (CO5)**

6. Design a hazards- free asynchronous circuit that changes state whenever the input goes from logic 1 to logic 0.**(JUNE 2013) (CO5)**

7.As asynchronous sequential circuit is described by the following excitation and output function

y = x_1x_2+(x_1+x_2)y   z = y   i) Draw the logic diagram of the circuit and describe the behaviour of the circuit. ii) Derive the transition table and output map. **DEC2008 (CO5)**

8. Find a static and dynamic hazard free realization for the following function using NAND and NOR gates. F(a, b, c, d) = $\sum$m(1,5,7,14,15) **APRIL/MAY 2011(CO5)**

9. Design a pulse mode circuit with three inputs x1, x2, x3 and one output z. The output z should change from 0 to 1, only for the input sequence x1-x2-x3.Also the output z should remain in 1 until x2 occurs. Use SR flip flop for the design. **(DEC 2013). (CO5)**

10.Discuss on hardware description language. (Dec 2013/Jan 2014) (Understanding) (CO5)