K.S.R. COLLEGE OF ENGINEERING, TIRUCHENGODE – 637 215.
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
COURSE / LESSON PLAN SCHEDULE

NAME : T.M.SATHISH KUMAR
CLASS : III ECE A & B
SUBJECT : 16EC614 -VLSI DESIGN

A.TEXT BOOKS :

1. John P Uyemura- **"Chip Design for Submicron VLSI: CMOS layout and simulation"** Thomson India Edition- 2006.
2. Samir Palnitkar, **"Verilog HDL A Guide to Digital Design and Synthesis"**, 2nd edition, Pearson Education, 2008.

B. REFERENCE:

1. Neil H.E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", Pearson Education Asia, 2nd edition, 2005.
2. Kamran Eshraghian, Douglas A. Pucknell and Sholeh Eshraghian, "Essentials of VLSI Circuits and Systems", Prentice Hall of India Pvt Ltd, 2013.
3. Wayne Wolf, "Modern VLSI Design System-On-Chip", PHI, 3rd edition, 2007.
4. John P. Uyemura, "Introduction to VLSI Circuits and Systems", John Wiley & Sons, 2002.
5. J.Bhasker, "Verilog HDL Primer", BS publication, 2002.

C. LEGEND:

L 1 - Lecture 1 BB - Block Board
OHP - Over Head Projector LCD - Liquid Crystal Display
Tx 1 - Text 1 Rx 1 -Reference 1 pp - Pages

Sl.No	Lecture Hour	Topics to be covered	Teaching Aid Required	Book No. / Page No.
UNIT-I MOS TECHNOLOGY				
1	L1	Chip Design Hierarchy	BB	Tx1/pp17-20
2	L2	IC Layers	BB	Tx1/pp20-24
3	L3	Photolithography and Pattern Transfers	BB/LCD	Tx1/pp24-28
4	L4	CMOS Fabrication (nWell - pWell - Twin tub - Silicon on insulator)	BB/LCD	Tx1/pp43-52
5	L5	Submicron CMOS Process	BB	Tx1/pp52-54
6	L6	Masks and Layout	BB	Tx1/pp57-61
7	L7, T1	Types of rules :CMOS Design Rules	BB/LCD	Tx1/pp85-87
8	L8, T2	SCMOS Design Rule set	BB	Tx1/pp88-96
9	L9	Lambda based layout	BB/LCD	Tx1/pp66-69
UNIT-II MOSFET TRANSISTOR				
10	L10	Basic MOS Transistors	BB	Tx1/pp39-43
11	L11	MOSFET operation	BB/LCD	Tx1/pp108-119
12	L12	MOSFET switch model and square law model	BB	Tx1/pp119-121 Tx1/pp121-126
13	L13	MOSFET parasitics	BB	Tx1/pp126-131
14	L14	MOSFET SPICE Modeling	BB	Tx1/pp134-142
15	L15	CMOS Inverter Voltage Transfer curve	BB/LCD	Tx1/pp157-169 Tx1/pp159

16	L16	Body Effect, Threshold voltage	BB	Rx1/pp47-51
17	L17	Latch up problem in CMOS circuits	BB	Rx1/pp157-160
18	L18	Latch up prevention	BB	Rx1/pp161-163
UNIT-III CMOS LOGIC GATES DESIGN AND LAYOUT				
19	L19, T3	NAND and NOR Gates	BB/LCD	Tx1/pp169-182
20	L20, T4	Complex Logic Gates	BB/LCD	Tx1/pp183-186
21	L21, T5	Stick Diagram	BB/LCD	Rx2/pp 3-43
22	L22, T6	CMOS Layout	BB/LCD	Tx1/pp169-182
23	L23	Tri state circuits	BB	Tx1/pp189-190
24	L24	Large FETs	BB	Tx1/pp190-193
25	L25, T7	Transmission Gate and Pass Transistor Logic	BB	Tx1/pp193-197
26	L26	Standard Cell design- Cell hierarchies	BB/LCD	Tx1/pp198-207
27	L27	Cell libraries	BB/LCD	Tx1/pp207-213
UNIT-IV STORAGE ELEMENTS AND DYNAMIC LOGIC CIRCUITS				
28	L28	SR Latch	BB	Tx1/pp221-224
29	L29	Bit Level Register	BB	Tx1/pp224-227
30	L30	D Flip Flop	BB	Tx1/pp227-228
31	L31	Dynamic D Flip Flop	BB	Tx1/pp228-231
32	L32	Static RAM Cell	BB	Tx1/pp231-235
33	L33, T8	Clocked CMOS, Dynamic Logic	BB	Tx1/pp237-241
34	L34	Domino Logic	BB	Tx1/pp241-244
35	L35	SR Logic	BB	Tx1/pp244-246
36	L36	Dynamic Memories	BB	Tx1/pp246-249
UNIT- V Verilog HDL				
37	L37	Basic concepts	BB	Tx2/pp91-101
38	L38	Modules and ports	BB	Rx4/pp371-373
39	L39, T9	Structural Gate Level modeling	BB	Tx2/pp105-123 Rx4/pp373-383 Rx5/pp83-102
40	L40, T10	Data flow modeling	BB	Tx2/pp131-156
41	L41, T11	Behavioral Modeling	BB	Tx2/pp161-207 Rx4/pp392-399
42	L42, T12	Switch Level Modeling	BB	Tx2/pp277-289 Rx4/pp383-388
43	L43, T13	Test benches ,Gate Level description of Adders, Subtractor	BB	Tx2pp/60-66,113-120,147-152,201-203
44	L44, T14	Multiplexer, Demultiplexer, Encoder, Decoder	BB	
45	L45, T15	Comparator, Priority Encoder, D Latch and D Flip Flop, Shift Register and Counter	BB	

FACULTY INCHARGE **HOD/ECE**

VLSI DESIGN

UNIT I – MOS TECHNOLOGY (CO1)

2 MARKS:

1. **What is design hierarchy? What are its types? (Remembering)** (June 16)
   Integrated circuits are quite complex in designing and fabricating, the task is made easier by breaking the problem into design hierarchy where problem is viewed at different levels. Types of designs are system design, logic design, circuit design, and physical design and chip design.
2. **What is IC? What are different IC layers? (Remembering)**
   Integrated Circuit (ICs) are microscopic electronic networks that are created in a special type of material called a semiconductor. Silicon is a semiconductor which is used as a base material for majority of modern electronic system. Base or substrate, Oxide layer, SiO_2 (insulating) layer, metal layer (contact or via) are some of IC layers.
3. **What is meant by photolithography? (Remembering)** (Nov/Dec 11) (June 16)
   Photolithography is an important processing step involved in IC fabrication; it is used to create patterned material layers to guide electrical signals on the chip. Photo masking and photo etching are the two key process involved in photolithography for making patterned materials.
4. **What is RIE? (Remembering)** (May/June 10)
   RIE is Reactive Ion Etching in which ionized atoms of an inert gas such as argon (Ar) are mixed with etching assisting chemicals. The mixture is then excited with a radio frequency (rf) electric field in a manner that drives the ions/chemicals in a vertical up-down motion to etch away the surface.
5. **What is feature size? (Remembering)**
   Feature size or minimum feature size of an IC is the smallest dimension that can actually be transferred to a chip.
6. **What is meant by submicron and deep submicron? (Understanding)**
   Modern facilities can manufacture chips with minimum feature sizes smaller than 1 micron which is known as submicron technique. Advanced state of art fabrication plants can produce integrated circuits where the smallest feature size is less than 0.1 µm wide which is called deep submicron technique.
7. **Define Aspect Ratio. (Remembering)**
   It is the ratio between channel width (W) and channel length (L). Aspect ratio = W/L
8. **Draw the symbol of nFET and pFET. (Understanding)**

9. **Define threshold voltage. (Remembering)**
   The Threshold voltage, V_T for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, I_{DS} effectively drops to zero. Threshold voltage is the voltage at which the device turns on or starts conducting.
10. **What is self aligned technique? (Remembering)**
    In the MOSFET fabrication process, gate and n+ or p+ regions automatically aligned to each other which is known as self aligned technique.
11. **What is CMP? (Remembering)**
    Planarization is mandatory in chips that use more than two or three metal layers. The most common technique is Chemical-Mechanical Polishing (CMP) which is capable of producing very flat surfaces.
12. **What is meant by doping? List some of dopants. (Remembering)**
    The process of adding impurity atoms is called doping. Impurities themselves are called dopants, e.g. - arsenic and silicon.
13. **What is LDD? (Remembering)** (Nov/Dec 10)
    LDD is Lightly Doped Drain structure. This structure is used to reduce some small device effect due to very energetic partials called hot electrons and hot holes.
14. **What are generations of Integration Circuits? (Remembering)**
    SSI (Small Scale Integration), MSI (Medium Scale Integration) , LSI (Large Scale Integration) , VLSI (Very Large Scale Integration) , ULSI (Ultra Large Scale Integration , GSI(Giga Scale Integration).
15. **Give the basic process for IC fabrication. (Remembering)**

Silicon wafer Preparation, Epitaxial Growth, Oxidation, Photolithography, Diffusion, Ion Implantation, Isolation technique, Metallization, Assembly processing & Packaging.

16. **What are the different layers in MOS transistors? (Remembering) -** Drain, Source & Gate
17. **Give the different types of CMOS process? (Remembering)**
    P-well process, N-well process, Silicon-On-Insulator Process, Twin- tub Process.
18. **What are the steps involved in twin-tub process? (Remembering)**
    Tub Formation, Thin-oxide Construction, Source & Drain Implantation, Contact cut definition, Metallization.
19. **What are the advantages of CMOS process? (Remembering)**
    Low power Dissipation, High Packing density, Bi directional capability, Low Input Impedance, Low delay Sensitivity to load.
20. **What is pull down device? (Remembering)**
    A device connected so as to pull the output voltage to the lower supply voltage usually 0V is called pull down device. nMOS is good for logic '0' so it is known as pull down device.
21. **What is pull up device? (Remembering)**
    A device connected so as to pull the output voltage to the upper supply voltage usually V_{DD} is called pull up device. pMOS is good for logic '1' so it is known as pull up device.
22. **What are the common materials used as mask? (Remembering)**
    Photoresist, twin dioxide (SiO_2), Polisilicon (polycrystalline silicon), Silicon nitrate (SiN).
23. **What is Stick Diagram? What are its uses? (Understanding)**
    It is used to convey information through the use of color code. Also it is the cartoon of a chip layout. It can be drawn much easier and faster than a complex layout. These are especially important tools for layout built from large cells.
24. **Give the various color coding used in stick diagram? (Remembering)**
    Green – n-diffusion, Red- polysilicon, Blue –metal, Yellow- implant, Black-contact areas.
25. **What are design rules?(maj/june 2014) (Remembering)**
    Design rules are the communication link between the designer specifying requirements and the fabricator who materializes them. Design rules are used to produce workable mask layouts from which the various layers in silicon will be formed or patterned.
26. **What is Lambda (λ) - based design rules? (Remembering)**
    These rules popularized by Mead and Conway are based on a single parameter λ, which characterizes the linear feature – the resolution of the complete wafer implementation process and permits first order scaling. They have been widely used, particularly in the educational context and in the design of multi project chips. In lambda based design rules, all paths in all layers will be dimensioned in λ units and subsequently λ can be allocated an appropriate value compatible with the feature size of the fabrication process. Design rules; specify line widths, separations, and extensions in terms of λ.
27. **State any two differences between CMOS and Bipolar technology. (Understanding)**

CMOS Technology	Bipolar technology
• Low static power dissipation	• High power dissipation
• High input impedance (low drive current)	• Low input impedance
• Scalable threshold voltage	(high drive current)
• High noise margin	• Low voltage swing logic
• High packing density	• Low packing density
• High delay sensitivity to load	• Low delay sensitivity to load
• Low output drive current	• High output drive current
• Low gm (gm a Vin)	• High gm
• Bidirectional capability	• High ft at low current
• A near ideal switching device	• Essentially unidirectional

28. **List any two types of layout design rules. (Remembering)(**Dec 2015),(Nov/Dec 11)
    λ- rule , μ- rule.
29. **What are the major types of design rules? (Remembering)** (May/June 12)
    Major types of design rules are minimum feature rule, minimum spacing rule, surround rule and exact size rule.
30. **What is the max contact width of metal1 line with active poly? (Remembering)** (Nov/Dec 11) **,**3λ
31. **Define yield.(Remembering)**(May/June 10)

Fraction (or percentage) of good chips produced in a manufacturing process is called the yield. Yield is denoted by symbol *Y*.

32. State Moore's law (Remembering) (June 15)

"Moore's law" is the observation that, over the history of computing hardware, the number of transistors in a dense integrated circuit has doubled approximately every two years.

33. Mention the advantages of SOI process (Remembering) (June 15)

Reduced Source and Drain to Substrate Capacitance.
Absence of Latchup.
Lower Passive current.
Denser Layout → Low cost

34. What are the advantages of twin-tub process (Dec 2015)

- Can optimize NMOS and PMOS transistors separately.
- Transistor parameters such as threshold voltage, body effect and the channel transconductance of both types of transistors can be tuned independently
- Problem of unbalanced drain parasitic is solved

BIG QUESTIONS:

1. Explain design hierarchy with neat diagram. (Understanding) (Nov/Dec 15)
2. Explain in detail about photolithography and pattern transfers. (Understanding) (June 15)
3. Describe the basic MOS transistor operation. (Understanding)
4. Explain the CMOS fabrication technique with neat diagram. (Understanding)(May/June 10)
5. With neat diagrams explain the steps involved in the p-well fabrication process. (Understanding) (June 15) (Nov/Dec 11)
6. With neat diagrams explain the steps involved in the n-well fabrication process. (Understanding) (Nov/Dec 10) (June 16)
7. Describe in detail with neat sketches the Twin Tub method of CMOS fabrication. (Understanding)
8. Explain with neat diagram the SOI process and mention its advantages. (Understanding) (Nov/Dec 15)
9. Explain in detail about submicron CMOS process. (Understanding)
10. Explain the construction and operation of nMOS and pMOS enhancement mode transistor. (Understanding) (May/June 10) (Dec 2015)
11. Explain the operation of pMOS depletion mode transistor. (Understanding)
12. Explain in detail about CMOS design rules. (Understanding)
13. Write notes on lamda based layout rule. (Understanding)(June 15)
14. Discuss in detail about different SCMOS design rule set. (Understanding) (June 15)(Dec 2015)
15. Draw the layout of CMOS inverter.(Understanding)(Nov/Dec 11)
16. List the sequence of steps to create the pattern. (Understanding)(May/June 12)
17. Describe SCMOS design rule set with examples. (Remembering) (June 16)
18. Illustrate submicron CMOS process. (Understanding) (June 16)

UNIT II – MOSFET (CO2)

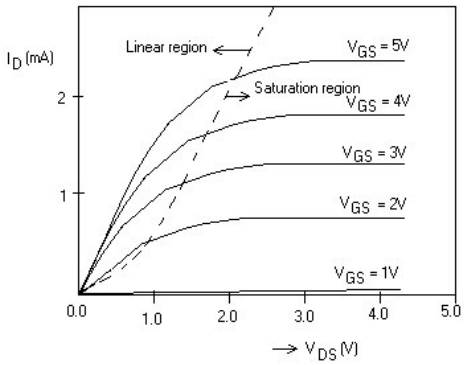
2 MARKS:

1. What is MOSFET? What are their advantages? (Remembering)

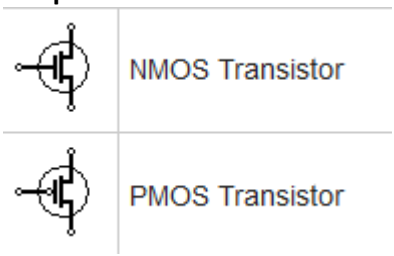
Metal Oxide Semiconductor Field Effect Transistor (MOSFET) provide all of the switching and amplifications in the CMOS integrated circuits. The speed of a digital chip is directly related to the electrical characteristics of the transistors, which are in turn functions of the layout and processing technology.

2. What are the different operating regions for an MOS transistor? (Understanding)

Cutoff region, Non- Saturated Region, Saturated Region



3. **Draw the symbol of pMOS and nMOS transistor. (Understanding)**



4. **What is surface geometry? (Remembering)**

The current flow through a MOSFET is controlled by the voltages, but the surface geometry plays a major role in how much current the device can conduct. Channel width (W) is the most important dimension.

5. **Write the equation for device and process Transconductance. (Understanding)**

$$\beta_n = k_n'(W|L)_n \, , \qquad k_n' = \mu_n C_{ox}$$

Where β_n - Device conductance and has unit of A/V^2

k_n' - Process conductance and has unit of A/V^2

μ_n - Mobility, C_{ox}- Oxide capacitance, W-channel width, L-channel length

6. **What is mobility ratio? (Remembering)**

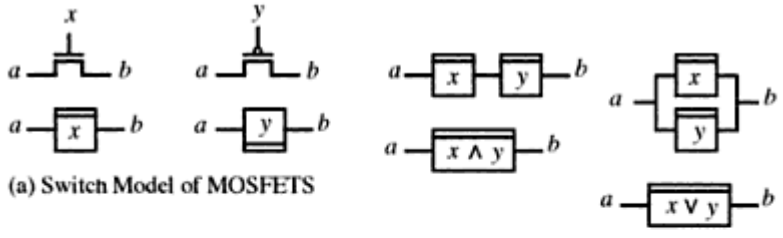
The ratio of process conductance equations of n and p device is called mobility ratio(r).

$$\frac{k_n'}{k_p'} = \frac{\mu_n C_{ox}}{\mu_p C_{ox}} = r$$

7. **What is complementary pair? (Remembering)**

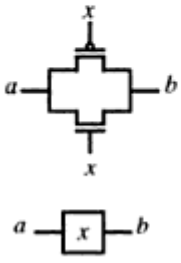
In CMOS logic nFET and pFET are used in pairs with a common gate input which is known as complementary pair.

8. **Draw the nMOSFET, pMOSFET switching models.(Understanding)**(Nov/Dec 11)



(a) Switch Model of MOSFETS

(b) Series and Parallel Combinations



(c) Complementary Pass Gate

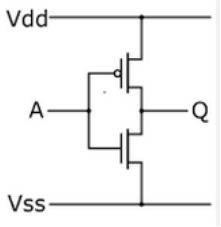
9. **What is square law model? (Remembering) (Dec 2015)**

Square law model is the simplest analytical model of MOSFET which is used to compute currents from device voltages using closed-form equations.

10. **What are the types of regions available in square law model analysis? (Remembering)**

Cutoff region, Triode region and Saturation region.

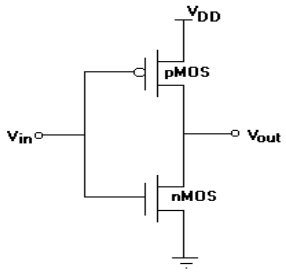
11. Draw CMOS complementary pair. (Understanding)



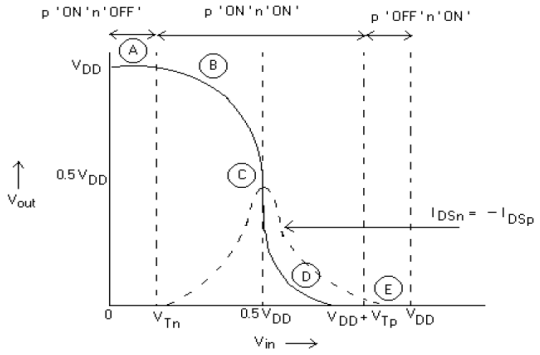
12. What are parasitic components? (Remembering)

Parasitic components are some unwanted components i.e., transistors, resistors, capacitors that are formed during the fabrication of a device.

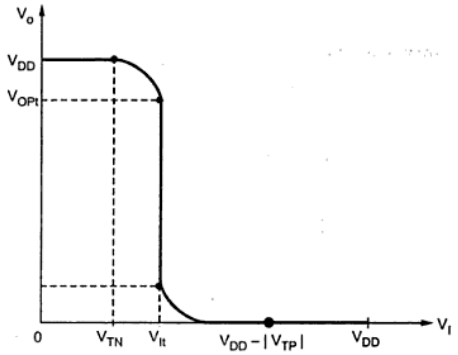
13. Draw the circuit of a CMOS inverter. (Understanding)



14. Give the CMOS inverter DC transfer characteristics and operating regions(Understanding)



15. Draw VTC of CMOS inverter. (Understanding)



16. What are the different regions of operation of a MOS transistor? (Remembering)

a. Cut off region :Here the current flow is essentially zero (accumulation mode)
b. Linear region: It is also called weak inversion region where the drain current is dependent on the gate and the drain voltage w. r. to the substrate.
c. Saturation region: Channel is strongly inverted and the drain current flow is ideally independent of the drain-source voltage (strong-inversion region).

17. Give the expressions for drain current for different modes of operation of MOS transistor. (Understanding)

a. Cut off region: $I_D = 0$
b. Linear region: $I_D = k_n [(V_{GS} – V_T) V_{DS} – V_{DS}^2/2]$
c. Saturation region: $I_D = (k_n /2) (V_{GS} – V_T)^2$

18. What are the secondary effects of MOS transistor? (Remembering)

Threshold voltage variations, Source to drain resistance, Variation in I-V characteristics, Sub threshold conduction, CMOS latchup.

19. **Define Threshold voltage in MOS? (Remembering)** (Dec 2015)

The Threshold voltage, V_T for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, I_{DS} effectively drops to zero.

20. **What is Body effect? (Remembering)** (June15)(Nov/Dec11) (May/June 12) (June 16)

The threshold voltage V_T is not a constant w. r. to the voltage difference between the substrate and the source of MOS transistor. This effect is called substrate-bias effect or body effect.

21. **What is Channel-length modulation? (Remembering)**

The current between drain and source terminals is constant and independent of the applied voltage over the terminals. This is not entirely correct. The effective length of the conductive channel is actually modulated by the applied V_{DS}, increasing V_{DS} causes the depletion region at the drain junction to grow, reducing the length of the effective channel.

22. **Define mobility variation (μ). (Remembering)**

$$\mu = \frac{Average\ carrier\ drift\ velocity\ (V)}{Electric\ field(E)}$$

23. **What is latch-up? (Remembering)** (Dec 2015)(May/June 12) (June 16)

In CMOS circuits the unwanted parasitic components will give raise to parasitic circuit effect called 'latch up'. The result of this effect is shortening of VDD and VSS lines, usually resulting in chip self destruction.

24. **How latch up can be prevented?(Understanding)**(Nov/Dec 11)

Latch up can be prevented by the following steps

1. By increasing substrate doping levels with a consequent drop in the value of R_{subs}.
2. By reducing R_{nwell} by control of fabrication parameters and ensuring a low contact resistance to VDD.
3. By introducing guard rings.

25. **What are the advantages of CMOS inverter over the other inverter configurations? (Understanding)**

a. The steady state power dissipation of the CMOS inverter circuit is negligible.
b. The voltage transfer characteristic (VTC) exhibits a full output voltage swing between 0V and V_{DD}. This results in high noise margin.

26. **What are the static properties of complementary CMOS Gates? (Understanding)**

a. They exhibit rails-to-rail swing with $V_{OH} = V_{DD}$ and V_{OL} = GND.
b. The circuits have no static power dissipation, since the circuits are designed such that the pull-down and pull-up networks are mutually exclusive.
c. The analysis of the DC voltage transfer characteristics and the noise margins is more complicated than for the inverter, as these parameter depend upon the data input patterns applied to the gate.

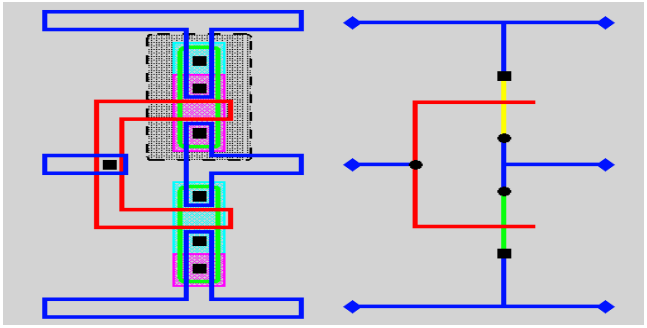
27. **Give the equation for PFET resistance R_P (Remembering)**(May/June 10)

28. **Write the level1 SPICE MOSFET parameters. (Remembering)**(May/June 10)

Electrical parameters for level 1 MOSFET SPICE model.

Electrical parameter	*Symbol used by SPICE*
K'	KP
V_{T0}	VT0
γ	GAMMA
$\|2\phi_F\|$	PHI
λ	LAMBDA

29. **Draw the Stick Diagram of CMOS Inverter. (Understanding)**(May/June 12)



30. Mention the significance of beta ratio of CMOS inverter (Remembering)(June 15)

BIG QUESTIONS:

1. Explain the MOSFET operation with neat diagram.(Understanding)(Nov/Dec 11)
2. Explain MOSFET switching models. (Understanding)
3. Derive square law model of a MOSFET. (Understanding) (May/June 12)
4. Discuss in detail about MOSFET capacitance model /parasitic.(June15/Dec15) (Understanding)
5. Explain in detail about analytical description of MOSFET. (Understanding)
6. Describe the MOSFET SPICE modeling. (Understanding)
7. Explain the electrical characteristics of CMOS inverter with neat diagram. (Understanding)
8. Draw the voltage transfer curve and explain the DC property of CMOS inverter. (Understanding)
9. What is body effect? Explain in detail. (Understanding) (Dec 2015)
10. Derive the expression for DC characteristics of CMOS inverter. (June 15/ Dec 15)(Apply)
11. What is latch up? Explain the methods to prevent latch up?(Understanding)(June 15)(Dec 15) (June 16)
12. Explain the following second order effect, (i) threshold voltage and body effect, (ii) Channel length modulation and mobility variation. (Understanding)(Nov/Dec 10)
13. Derive DC transient characteristics of CMOS inverter (Understanding). (June 15) (May/June 10) & (Nov/Dec 10)
14. How do you calculate the sheet resistance and area of capacitance for a MOSFET? (Applying) (Nov/Dec 11)
15. Explain the transfer characteristics of CMOS inverter in all regions with the necessary equations.(Applying) (Nov/Dec 11)
16. Explain the electrical characteristics that will affect the design of an integrated circuit. (Understanding)(May/June 12)
17. Derive the Ids and Vds relationship for a MOS transistor in all three regions of operation and draw the MOS transistor characteristics.(Understanding)(June 15)
18. Explain the large signal MOSFET model. (Understanding)(June 16)
19. Elaborate on the simulation of a circuit using SPICE with suitable flowchart. (Remembering)(June 16)
20. Construct the voltage transfer characteristics of CMOS inverter and explain the five regions of operation. (Understanding)(June 16)

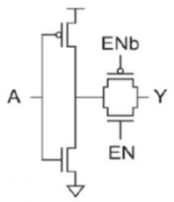
UNIT III – CMOS LOGIC GATES DESIGN AND LAYOUT (CO3)

2 MARKS:

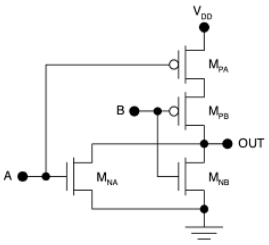
1. **What is a tri-state circuit? (Remembering)** (Nov/Dec 11)

   A standard logic gate has outputs of 0 and 1. In tri-state circuit, the output can also be in a Hi-Z (high impedance) state, giving three distinct states.

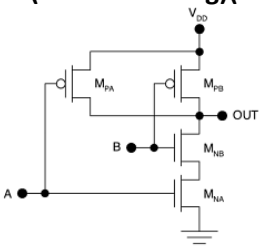
2. **Draw the diagram of tri-state inverter. (Understanding)**



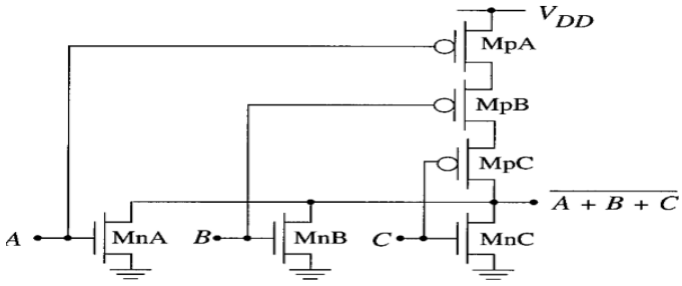
3. **Draw the CMOS NOR2 logic circuit. (Understanding)**



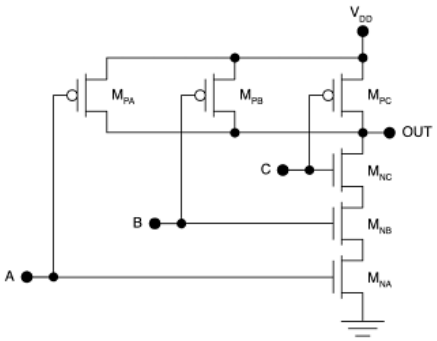
4. **Draw the CMOS NAND2 logic circuit. (Understanding)(June/Dec 15)**



5. **Draw the CMOS NOR3 logic circuit. (Understanding)**

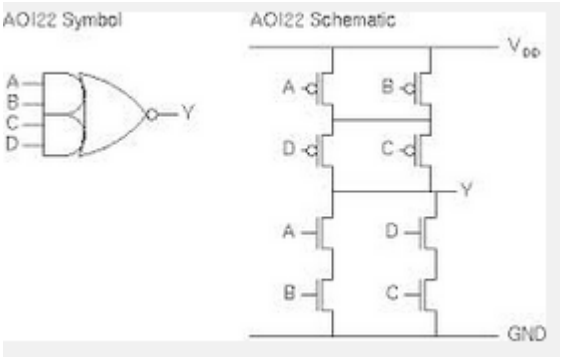


6. **Draw the CMOS NAND3 logic circuit. (Understanding)**

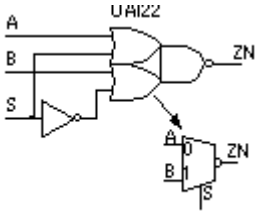


7. **Define rise time and fall time. (Remembering)**
   Rise time- it is the time for signal to rise from a low value to the high value in a linear ramp.
   Fall time- it is the time interval for the pulse to fall from a high to a low value.
8. **Define time start and time pulse. (Remembering)**
   Time start- it is the delay from t=0 before the pulse is applied. **Time pulse**- it is the pulse width, i.e., the length of time that the pulse is kept at the high value.

9. **What are complex logic gates? (Remembering)**
   Complex logic gates give a combination of logical OR and AND functions in a single circuit. This CMOS feature is quite useful for merging functions and designing small circuits.
10. **Draw the AOI22 logic circuit. (Understanding)**



11. Draw the OAI22 logic circuit. (Understanding)



12. Define rise time and fall time. (Remembering) (Nov/Dec 08) & (April/May 08)

Rise time t_r is the time for a wave form to rise from 10%to 90% of its steady state value. Fall time t_f is the time for a waveform to fall from 90% to 10% of its steady state value.

13. What is FET? (Remembering)

The field effect transistor (FET) is a semiconductor device in which current is controlled by an electric field. The operation of FET is depends on the flow of majority carriers only, so it is known as unipolar device.

14. What are large FETs? (Remembering)

Large FETs are FETs with large channel widths (W). The channel with (W) will be large compared to the channel length (L), so that device can accommodate large current levels.

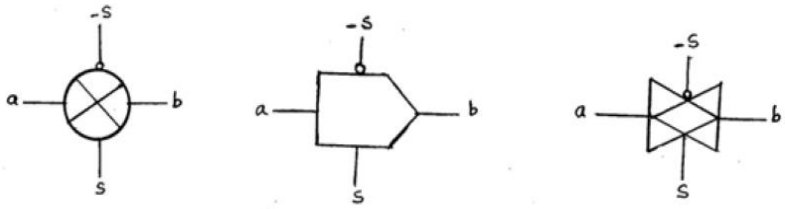
15. What is drift current? (Remembering)

Drift current is a current produced due to the movement of electrical charges under the influence of electric field. FETs conduct electricity using drift current.

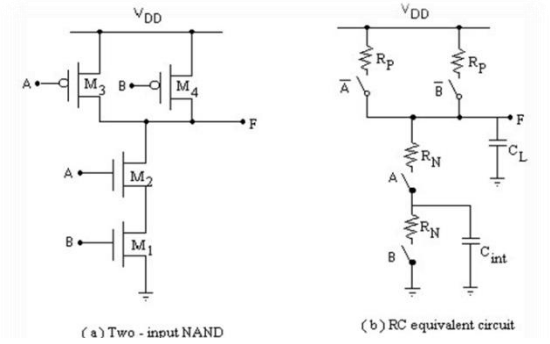
16. What is a transmission gate (TG)? (Remembering)

A transmission gate is a parallel connected nFET/pFET pair that acts as a logic switch.

17. Give the different symbols for Transmission Gate (TG). (Understanding)



18. Draw the equivalent RC model for a two-input NAND gate. (Understanding)



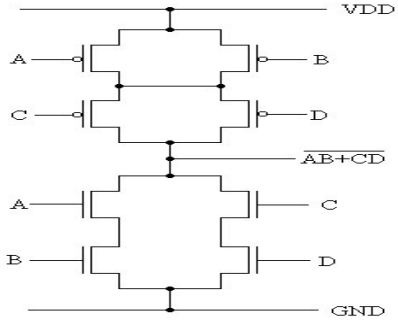
19. What is standard cell design? (Remembering)

High-density digital VLSI systems are created from primitive components using the concepts of repetition and structural regularity. Standard cell design is an approach that uses a collection of logic cells to create more complex networks.

20. Give the steps in ASIC design flow. (Remembering)

Design entry, Logic synthesis System partitioning, Pre layout simulation, Floor planning, Placement, Routing, Extraction, Post layout simulation.

21. Draw the static AOI CMOS gates to realize Y=(AB+CD) (Understanding)



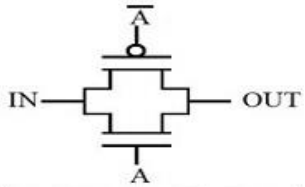
22. What is ASIC? Give the different types of ASIC. (Remembering)

ASIC is Application Specific Integrated Circuit.1.Full custom ASICs,2. Semi-custom ASICs,2.a.Standard cell based ASICs,2.b.Gate-array based ASICs,3.Programmable ASICs,3.a.Programmable Logic Device (PLD), 3.b.Field Programmable Gate Array (FPGA).

23. What is a FPGA? (Remembering)

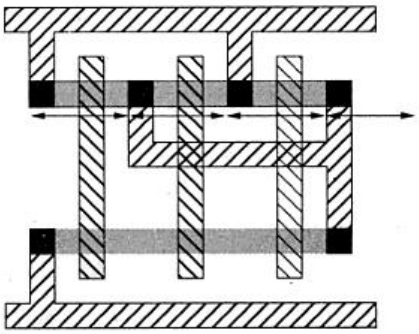
A field programmable gate array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of up to about 20,000 equivalent gates.

24. Give the principle and operation of transmission gate.(Understanding)(June 16)

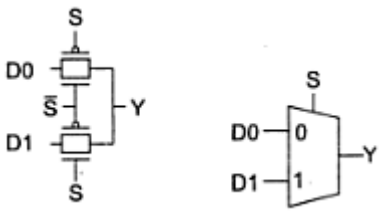


CONTROL		INPUT	OUTPUT
pMOS	nMOS	IN	OUT
0	1	0	0
		1	1
1	0	0	Z
		1	

25. Draw the layout of two input NAND gate.(Understanding)(Nov/Dec 11)



26. Design 2:1 MUX using Transmission Gate. (Understanding) (May/June 12)



27. Define Logical Efforts. (Remembering) (May/June 12)

Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current.

28. What is charge leakage? (Remembering) (May/June 12)

The charge storage on the capacitor C is subject to a problem called charge leakage that exists in CMOS circuits .This is due to unwanted conduction paths, like sub threshold and reverse pn-junction currents that cannot be eliminated.

29. **Define retention time. (Remembering)** (May/June 12)
The hold time t_h is the longest time that a logic 1 can be maintained in the cell; this is known as the retention time
30. **List the various forms of CMOS logic structures**. **(Remembering)**(June 15)
    - Dynamic CMOS Logic
    - CMOS Domino Logic
    - Pass-Transistor Logic
    - BiCMOS Logic
    - Clocked CMOS Logic (C^2 MOS)
    - NP Domino Logic (Zipper CMOS)
    - Cascade Voltage Switch Logic (CVSL)
    - Source Follower Pull-up Logic (SFPL)
31. **Differentiate pass transistor and transmission gate.(Understanding)**(Nov/Dec 15)
32. **List the advantages of using pass transistor logic. (Remembering)**(June 16)
    - It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors.
    - Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages.

BIG QUESTION:

1. Discuss in detail about the serial and parallel connected FETs. (Understanding)
2. Explain how NOR and NAND gates are implemented using serial and parallel connected FETs. (Understanding)
3. Draw the NOT-Buffer combination circuit and explain its operation. (Understanding)
4. Explain how NOR3 and NAND3 gates are implemented. (Understanding)
5. Describe in detail about the complex logic gates and tri state circuit. (Understanding)
6. What is transmission gate and pass logic and explain in detail about the large FETs. (Understanding)
7. Design 2:1 MUX and XOR using TG.(Applying)(June /Dec15)
8. Explain in detail about cell hierarchy and standard cell design and cell libraries. (Nov/Dec 11) (Understanding)
9. Design XOR cell, half adder and full adder and explain the concept of cell hierarchy. (Understanding)
10. Explain in detail about cell entries. (Understanding)
11. Draw the Euler graph for the function F=(A+B+C).D (Understanding)(Nov/Dec 15)
12. Draw the logic circuit diagram of a 4:1 multiplier using (i) pass transistor, (ii) Transmission gate (Understanding) (Nov/Dec 11)
13. Realize 2 input XOR gate using CMOS transistor. (Understanding) (Nov/Dec 11)
14. Discuss the method of obtaining the physical layout of CMOS NOR gate(Applying) (June15)
15. Briefly discuss pass Transistor logic and Tristate inverter(Remembering)(June 15/Dec 15)
16. Write short notes on floor planning. (Dec 2015)
17. Construct an AOI CMOS equivalent for the sum of product expression, Y=ABD+DE+EFG. (Applying) (June 16)
18. Describe the structure of a standard cell design. (Understanding) (June 16)
19. Elaborate on (i) Cell hierarchy (ii) Cell libraries. (Remembering) (June 16)

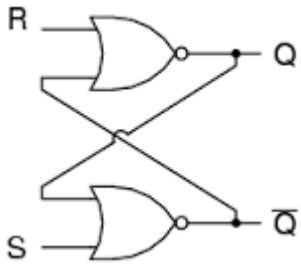
UNIT IV – STORAGE ELEMENTS AND DYNAMIC LOGIC CIRCUITS (CO4)

2 MARKS:

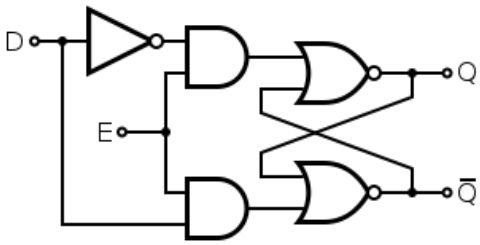
1. **What is called latch? (Remembering)**
   Latch is a simple memory element, which consists of a pair of logic gates with their inputs and outputs inter connected in a feedback arrangement, which permits a single bit to be stored.
2. **List different types of flip-flops. (Remembering)**
   SR flip-flop,Clocked RS flip-flop,D flip-flop,T flip-flop,JK flip-flop,JK master slave flip-flop.
3. **What do you mean by triggering of flip-flop.(Understanding)**

The state of a flip-flop is switched by a momentary change in the input signal. This momentary change is called a trigger and the transition it causes is said to trigger the flip-flop.

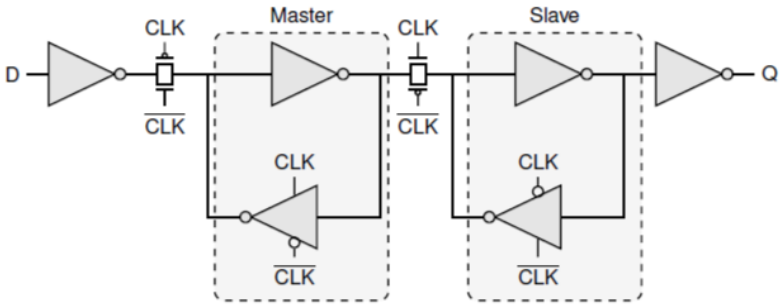
4. **What is an excitation table? (Remembering)**
   During the design process we usually know the transition from present state to next state and wish to find the flip-flop input conditions that will cause the required transition. A table which lists the required inputs for a given chance of state is called an excitation table.
5. **What is the operation of D flip-flop? (Remembering)**
   In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset.
6. **What is a master-slave flip-flop? (Remembering)**
   A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.
7. **Define registers. (Remembering)**
   A register is a group of flip-flops flip-flop can store one bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.
8. **Define Static RAM and dynamic RAM(Understanding)**
   Static RAM use flip flops as storage elements and therefore store data indefinitely as long as dc power is applied. Dynamic RAMs use capacitors as storage elements and cannot retain data very long without capacitors being recharged by a process called refreshing.
9. **Define flip-flop(Remembering)**
   Flip - flop is a sequential device that normally samples its inputs and changes its outputs only at times determined by clocking signal.
10. **Draw the NOR based SR latch, D-latch circuit, TG D-latch circuits. (Understanding)(June 15)**



SR latch



D latch

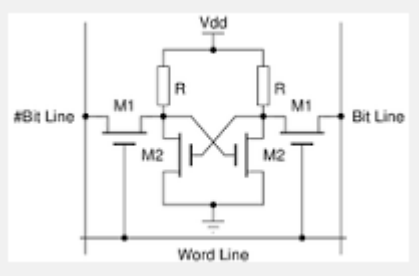


TG based D Latch

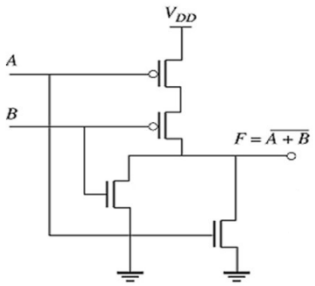
11. **What is SRAM? (Remembering)**
    Static Random Access Memories (SRAMs) are highly repetitive VLSI structures that are used for read/write data storage. An SRAM cell is different from a simple latch, in that it uses the same lines for input and output.
12. **What is a dynamic circuit? (Remembering)**
    A dynamic circuit operates by using the parasitic capacitance on a CMOS node to store electric charge.
13. **How dynamic flip-flop can be built? (Understanding)**
    A dynamic flip-flop can be built using two oppositely phased tri-state inverters.
14. **What is use of access transistors? (Remembering)**

Access transistors are used to provide conduction path to the internal bit storage circuit.

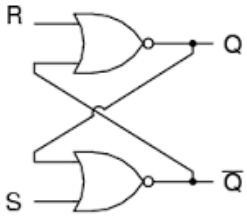
15. **What is domino logic? (Remembering)**
    Domino logic is an extension that adds an inverter at the output to overcome the hardware glitch.
16. **Draw SRAM cell. (Understanding)**



17. **What is SR logic? (Remembering)**
    The domino circuit is designed to use the clock pulse to synchronize the precharge event. Self-resetting logic (SR logic) uses a feedback network to automatically restore the charge on the internal capacitor after a discharge event.
18. **Dynamic NOR2 circuit. (Understanding)**

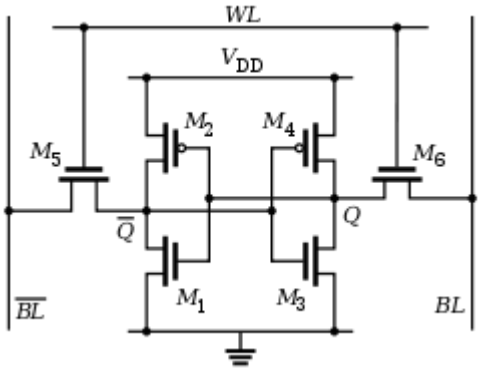


19. **Write the operational description table for SR latch. (Remembering)**



S	R	Q	$\overline{Q}$
0	0	latch	latch
0	1	0	1
1	0	1	0
1	1	0	0

20. **What are the advantages and applications of DRAM? (Remembering)**
    Dynamic RAMs (DRAMs) are most widely used memories because they can be manufactures at low cost at lowest cost per bit. System memories, such as those found in the motherboard of PC are DRAMs.
21. **What is ring oscillator? (Remembering)**(May/June 10)
    A ring oscillator is a device composed of an odd number of NOT gates whose output oscillates between two voltage levels, representing true and false. The NOT gates, or inverters, are attached in a chain; the output of the last inverter is fed back into the first.
22. **What is the hold time of dynamic memories? (Remembering)(June 15)**
    Hold time is defined as the minimum amount of time after the clock's active edge during which data must be stable. Violation in this case may cause incorrect data to be latched, which is known as a hold violation.
23. **List the gates in cell library(Dec 2015)**
    NAND,NOR,NOT,XOR
24. **Sketch the diagram of 6T SRAM cell. (Remembering)(June 16)**



BIG QUESTIONS:

1. What is latch? Explain in detail about its types and operation. (Understanding)
2. Explain in detail about bit level register. (Understanding)
3. Explain the operation of SR-latch and D-latch. (Understanding)
4. What is flip flop? Explain the operation of master-slave D-flip flop in detail. (Understanding)(June 15)
5. Draw the architecture of dynamic DFF and Explain in detail. (Remembering)(June/Dec 15)
6. Explain the read and write operations of static RAM cell with a CMOS circuit diagram. Draw its layout. (Understanding)(June/Dec 15)
7. Explain in detail about dynamic logic and domino logic.(Dec 2015) (Understanding)
8. Write notes on SR logic and DRAMs. (Understanding)
9. Explain read, write and hold operations performed by using CMOS SRAM cell. (Understanding) (Nov/Dec 10)
10. Explain the functions of static RAM cell with its SPICE simulation. (Understanding) (May/June 10)
11. Explain briefly about the structure of dynamic RAM cell. How the read, write, hold and refresh operations take place in a DRAM cell. (Understanding) (Nov/Dec 11)
12. Design two input AND gate using DOMINO logic. Also explain how domino logic is cascaded with different function (Remembering)(June 15)
13. Elucidate the problem of cascading in dynamic logic circuits. How can it be overcome? (Remembering)(June 16)
14. Explain the working of a dynamic D Flip flop. (Remembering)(June 16)
15. Compare static and dynamic CMOS logic circuits. (Understanding)(June 16)
16. Explain the operation of clocked CMOS logic circuit. (Understanding)(June 16)

UNIT V - VERILOG HDL (CO5)

1. **What are the various modeling used in Verilog? (Remembering)**
   Gate-level modeling, Data-flow modeling, Switch-level modeling, and Behavioral modeling
2. **What is the structural gate-level modeling**? **(Remembering)**
   Structural modeling describes a digital logic networks in terms of the components that make up the system. Gate-level modeling is based on using primitive logic gates and specifying how they are wired together.
3. **What is need for Verilog HDL? (Remembering)**
   Verilog is a Hardware Description Language (HDL). A Hardware Description Language is a language used to describe a digital system, for example, a microprocessor or a memory or simple Flip-Flop. This just means that by using a HDL one can describe any hardware (digital) at any level.
4. **What is Switch-level modeling?(MAY/JUNE 2014) (Remembering)**
   Verilog allows switch-level modeling that is based on the behavior of MOSFETs. Digital circuits at the MOS-transistor level are described using the MOSFET switches.
5. **What are identifiers? (Remembering)**
   Identifiers are names of modules, variables and other objects that we can reference in the design. Identifiers consists of upper and lower case letters, digits 0 through 9, the underscore character(_) and the dollar sign($). It must be a single group of characters. Examples: A014, a, b, in_o, s_out
6. **What are the value sets in Verilog? (Remembering)**
   Verilog supports four levels for the values needed to describe hardware referred to as value sets.

Value levels	Condition in hardware circuits
0	Logic zero, false condition
1	Logic one, true condition
X	Unknown logic value
Z	High impedance, floating state

7. Give the classifications of timing control? (Understanding)

Methods of timing control: 1.Delay-based timing control 2. Event-based timing control 3. Level-sensitive timing control

Types of delay-based timing control: 1. Regular delay control 2. Intra-assignment delay control 3. Zero delay control

Types of event-based timing control: 1. Regular event control 2. Named event control 3. Event OR control 4. Level-sensitive timing control

8. Give the different arithmetic operators?

Operator symbol	Operation performed	Number of operands
*	Multiply	Two
/	Divide	Two
+	Add	Two
-	Subtract	Two
%	Modulus	Two
**	Power (exponent)	Two

9. What are the types of procedural assignments?(DEC 2015) (Remembering)

1. Blocking assignment 2. Non-blocking assignment

10. What are gate primitives? (Remembering) (Dec 2015)

Verilog supports basic logic gates as predefined primitives. Primitive logic function keyword provides the basics for structural modeling at gate level. These primitives are instantiated like modules except that they are predefined in verilog and do not need a module definition. The important operations are and, nand, or, xor, xnor, and buf (non-inverting drive buffer).

11. Give the two blocks in behavioral modeling. (Remembering)

1. An initial block executes once in the simulation and is used to set up initial conditions and step-by-step data flow

2. An always block executes in a loop and repeats during the simulation.

12. Give the different bitwise operators. (Remembering)

Operator symbol	Operation performed	Number of operands
~	Bitwise negation	One
&	Bitwise and	Two
|	Bitwise or	Two
^	Bitwise xor	Two
^~ or ~^	Bitwise xnor	Two
~&	Bitwise nand	Two
~|	Bitwise nor	Two

13. What are the types of conditional statements? (Remembering)

1. No else statementSyntax: if ([expression]) true – statement;

2. One else statementSyntax: if ([expression]) true – statement;Else false-statement;

3. Nested if-else-ifSyntax: if ([expression1]) true statement 1;
if ([expression2]) true-statement 2;Else if ([expression3]) true-statement 3;
Else default-statement;The [expression] is evaluated. If it is true (1 or a non-zero value) true-statement is executed. If it is false (zero) or ambiguous (x), the false-statement is executed.

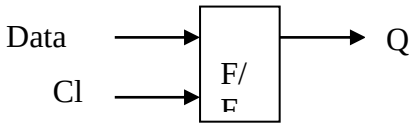
14. Name the types of ports in Verilog(Remembering)

Types of port	Keyword
Input port	Input
Output port	Output
Bidirectional port	inout

15. Why do you require sensitivity list. (Remembering) (Nov/Dec 08)

The sensitivity list indicates that when a change occurs to any one of elements in the list change, begin…end statement inside that always block will get executed.The list of events or signals expressed as an OR is known as a sensitivity list. A transmission on any one of multiple signals or events can trigger the execution of a statement or a block of statements .

16. **List out the classification of operators in verilog HDL. (Remembering)** (Nov/Dec 08)
    Types of operators are:
    Arithmetic,relational,equality,logical,bitwise,reduction,shift,conditional,concatenationand replication operators.
17. **Write the half adder program in verilog.(Nov/Dec 2011) (June 15) (Applying)**
    Module HA(s,c,a,b);Input a,b;Output s,c;xor (s,a,b);and (c,a,b);
    end module;
18. **Write the coding in verilog for the given block diagram. Use behavioural model. (Applying)**



    Module DFF (Q,D,clk);
    Input D,clk ;
    Output Q;
    reg Q;
    always @ (pos edge clk)
    Q=D
    end module;
19. **What is the difference between module and instance? (Understanding)**
    Module: basic building block
    Instance: an instance of module has a unique identity and is different from other instance of the same module. Each instance has an independent copy of internals of module.
20. **Give the need for switch level models? (Remembering)**
    Switch level models are used to allow detailed construction of logical gates and functions and also to allow complex delay modeling to be used.
21. **Give an example for implicit continuous assignments.(Nov/Dec 2012) (Applying)**
    Drive values to a net
    – assign out = a&b ; // and gate
    – assign eq = (a==b) ; // comparator
    – wire #10 inv = ~in ; // inverter with delay
    – wire [7:0] c = a+b ; // 8-bit adder
22. **Write the Verilog module for a 1 bit full adder. (Nov/Dec 2012) (Applying)**
    modulefa(a, b, c, sum, carry);
    input a,b,c;
    output sum,carry;
    wire d,e,f;
    xor(sum,a,b,c);
    and(d,a,b);
    and(e,b,c);
    and(f,a,c);
    or(carry,d,e,f);
    endmodule
23. **What are the delay specification available in Verilog HDL for modeling a logic gate**
    Specify propagation delay only (Nov/Dec 2011)
    gatename #(prop_delay) [instance_name](output, in_1,in_2,…);
    Specify both rise and fall times
    gatename #(t_rise, t_fall) [instance_name](output, in_1,in_2,…);
    Specify rise, fall, and turn-off times (tristate buffers)
    gatename #(t_rise, t_fall, t_off) [instance_name](output,in_1, in_2,…);
24. **Write the Verilog code to swap contents of two registers with/without a temporary register (May/June 2012)(Applying)**
    With temp reg ;
    always @ (posedge clock)begin
    temp=b;b=a;a=temp;end

Without temp reg;
always @ (posedge clock)begin a <= b;b <= a;end

25. **What are the difference between blocking and non-blocking assignments(Understanding)**
The Verilog language has two forms of the procedural assignment statement: blocking and non-blocking. The two are distinguished by the = and <= assignment operators. The blocking assignment statement (= operator) acts much like in traditional programming languages. The whole statement is done before control passes on to the next statement. The non-blocking (<= operator) evaluates all the right-hand sides for the current time unit and assigns the left-hand sides at the end of the time unit.

```
module blocking;
reg [0:7] A, B;
initial begin: init1
A = 3;
#1 A = A + 1; // blocking procedural assignment
B = A + 1;
$display("Blocking: A= %b B= %b", A, B ); A = 3;
#1 A <= A + 1; // non-blocking procedural assignment
B <= A + 1;
#1 $display("Non-blocking: A= %b B= %b", A, B );
end
endmodule
```

26. **What is VHDL? (Remembering)** (Dec 2006)
VHDL stands for Verilog Hardware Description Language. The design consists of module. A module start is a basic entity of the design. Module consists of design name and port list.
27. **What is meant continuous assignments in Verilog HDL? (Remembering)**
Continuous assignments are the most basic assignment in dataflow modeling. Continuous assignments are used to model in combinational logic. It drives values into the nets.
Simplified Syntax
net [strength] [range] [delay] identifier = net or register ;
assign [strength] [delay] net = net or register ;
28. **Give the design for defining the module? (Remembering)**

```
Module design_name (portlist);
Input list;
Output list;
Inout list;
Endmodule
```

29. **List out rules of identifiers? (Remembering)**

- ✓ Can contain alphanumeric or underscore characters or dollar sign.
- ✓ May use any character by escaping with a black Slash at beginning of the identifier and terminating with white space.
- ✓ Can be upto 1024 bytes
- ✓ Cannot contain white space

30. **What is the difference between === and == ? (Understanding)**
"==" it is logical equality.
"===" it is case equality.
output of "==" can be 1, 0 or X.
output of "===" can only be 0 or 1.
When you are comparing 2 nos using "==" and if one/both the numbers have one or more bits as "x" then the output would be "X" . But if use "===" outpout would be 0 or 1.
e.g A = 3'b1x0
B = 3'b10x
A == B will give X as output.
A === B will give 0 as output.
"==" is used for comparison of only 1's and 0's .It can't compare Xs. If any bit of the input is X output will be X
"===" is used for comparison of X also.

31. **What is the difference between wire and reg? (Understanding)**
    Net types: (wire,tri)Physical connection between structural elements. Value assigned by a continuous assignment or a gate output. Register type: (reg, integer, time, real, real time) represents abstract data storage element. Assigned values only within an always statement or an initial statement. The main difference between wire and reg is wire cannot hold (store) the value when there no connection between a and b like a->b, if there is no connection in a and b, wire loose value. But reg can hold the value even if there in no connection. Default values:wire is Z,reg is x.
32. **Mention the various operators in Verilog. (Remembering)**(June 15)

Arithmetic Operators	+, -, *, /, %
Relational Operators	<, <=, >, >=
Equality Operators	==, !=, ===, !==
Logical Operators	!, &&, ||
Bit-Wise Operators	~, &, |, ^, ~^
Unary Reduction	&, ~&, |, ~|, ^, ~^
Shift Operators	>>, <<
Conditional Operators	?:
Concatenations	{}

33. **Categorize the two blocks in behavioral modeling. (Understanding)** (June 16)
    Initial,Always
34. **Write the test bench for AND gate. (Creating)** (June 16)

```
module and_gate(
   input a,b,
   output y);
  assign y = a & b;
endmodule
```

TestBench

```
module tb_and_gate;
   reg A,B;
   wire Y;
   and_gate a1 (.a(A) ,.b(B),.y(Y));

   initial begin
      A =1'b0;
      B= 1'b0;
      #45 $finish;
   end
   always #6 A =~A;
   always #3 B =~B;
   always @(Y)
   endmodule
```

BIG QUESTIONS:

1. Explain the VLSI design flow with a neat diagram. (Understanding)
2. Explain the concept involved in structural gate level modeling and also give the description for half adder and Full adder. (Understanding)
3. Write a Verilog program for 3 to 8 decoder in gate level description. (Understanding) (Nov/Dec 08)
4. Write a Verilog program for 8 bit full adder using one bit full adder. The one bit full adder should be written in behavioral modeling. (Understanding) (Nov/Dec 08)
5. Explain in detail behavioral and RTL modeling. (Understanding) (Dec 2015)
6. Explain the syntax of conditional statements in Verilog HDL with examples. (April/May 08) (Understanding)
7. Write the structural gate level description of equality detector, comparator, priority encoder, D-latch, D flip flop,4 bit magnitude comparator(Understanding/Applying)
8. Explain the concept involved in Timing control in Verilog. (Understanding)

9. Write the program using Verilog HDL to implement a full adder circuit. (April/May 08) (Understanding)
10. With a neat flow chart explain the VLSI design flow. (Understanding) (April/May 08)
11. Explain gate level primitives and its design note. (Understanding)
12. Explain gate level modeling with suitable example (Understanding) (April/May 2011)
13. What are the main purposes of test benches (April/May 2011) (Understanding)
14. Write Verilog HDL coding for a decoder circuit Data flow and behavioral model (April/May11) (Understanding)
15. Draw the three input CMOS NOR and NAND gates and write the Verilog switch level modeling for both. (Nov/Dec 2011) (Understanding/Applying)
16. Explain the continuous and implicit continuous assignment with two suitable examples for each. (Understanding) (Nov/Dec 2011)
17. Draw the logic diagram of 4 to 1 MUX using NAND gates and write the gate level modeling using Verilog HDL. (Understanding/Applying) (Nov/Dec 2011)
18. Give a brief note on the looping statements available in Verilog HDL and write a verilog code for D Latch. (Understanding/Applying) (Nov/Dec 2011)
19. Draw an active high 2/4 decoder using NOR gates and write the Verilog gate level description.(Nov/Dec 2012) (Understanding/Applying)
20. Describe the 3 ways of specifying delays in continuous assignment statements.(Nov/Dec 2012) (Understanding)
21. Write the data flow modeling for a4:1 mux using Verilog HDL. (Understanding) (Nov/Dec 2012) (Understanding/Applying)
22. Explain the different timing controls available in Verilog HDL. (Understanding) (Nov/Dec 2012)
23. Give a Verilog HDL structural gate level description of a ripple carry adder (Dec 2007) (Understanding/Applying)
24. Write down the Verilog HDL description for combinational circuit. (June/Dec 2015, Apr/May 2011)(may/june 2014) (Understanding/Applying)
    (half subractor, full subractor, multiplexer, Demultiplexer, encoder, decoder, code conversion, Priority encoder, equality detector ,ripple carry adder.)
25. Write down the Verilog HDL description for sequential circuit. (May/June2010, Apr/May 2011) (Understanding/Applying)(Flip flops, counters, shift register, mealy, Moore machine, etc,)
26. Explain the various operators used in Verilog programming(Remembering)(June 15)
27. What is test bench and explain with one example(Remembering)(June 15)
28. Briefly discuss about Verilog operators(Dec 2015)
29. Explain the following with a suitable example. (Remembering)(June 16)
    (i) Timing controls and conditional statements in verilog.
    (ii) Behavioral and structural modeling in verilog
30. Develop the diagram of 4 to 1 MUX using NAND gates and write the gate level modeling using verilog HDL. (Creating) (June 16)
31. Elaborate on the looping statements available in verilog HDL and write the verilog code for D latch. (Creating) (June 16)

Reg. No. : 1 4 1 5 5 0 2

K.S.R. COLLEGE OF ENGINEERING, TIRUCHENGODE – 637 215

(AUTONOMOUS)

Question Paper Code : 171140

B. E. / B.Tech. DEGREE END SEMESTER EXAMINATION, DEC 2017 / JAN 2018

Sixth Semester

B.E. – ELECTRONICS AND COMMUNICATION ENGINEERING

12EC3604 – VLSI Design

(Regulations 2012)

Time: Three hours | Maximum Marks: 100

Answer ALL Questions

PART A — (10 x 2 = 20 Marks)

1. Compare nMOS and pMOS transistor.
2. Discuss the need of design rules.
3. Illustrate latch up condition in CMOS circuits? How to prevent it?
4. Define body effect and write the threshold equation including the body effect.
5. Develop a 2-input XOR gate using transmission gates.
6. What are the disadvantages of CMOS transmission gate? Draw its symbol.
7. Mention the drawbacks of dynamic logic.
8. Why single phase dynamic logic structure cannot be cascaded?
9. Compare blocking and non-blocking statement in Verilog HDL code.
10. Write a verilog code for half adder circuit.

PART B — (5 x 16 = 80 Marks)

11.(a) (i) Explain in detail CMOS fabrication technologies. (12)

(ii) Discuss about the lambda based design rules for NMOS and CMOS transistors. (4)

(Or)

(b) (i) Explain in detail about the ideal I-V characteristics of nMOS and pMOS devices. (8)

(ii) With neat diagram explain the n-well and channel formation in CMOS process. (8)

12. (a) (i) Explain the DC transfer characteristics of a CMOS inverter with necessary conditions for the different regions of operation (8)

(ii) Briefly explain about MOSFET parasitic. (8)

(Or)

(b) (i) Describe in detail about MOSFET switch model and square law model. (12)

(ii) Explain in detail about operation of MOSFET. (4)

13. (a) (i) Discuss in detail about the characteristics of CMOS transmission gate. (8)

(ii) Draw and explain about realization of inverters and basic gates using pass transistor logic. (8)

(Or)

(b) (i) With neat sketch, illustrate the operation of pass transistor DC characteristics. (12)

(ii) Design D-flip-flop using transmission gate. (4)

14. (a) (i) Describe the properties and operation of dynamic CMOS logic with neat diagram. (12)

(ii) Sketch a pseudo nMOS gate that implements the function Y= (A+B) (C+D). (4)

(Or)

(b) (i) Illustrate the operation of dynamic CMOS Domino and NP Domino logic with necessary diagrams. (8)

(ii) Briefly explain the difference between Static and Dynamic Memory. (8)

15. (a) (i) Briefly explain about different types of modeling present in Verilog HDL. (8)

(ii) Write the verilog code for 1:4 demultiplexer. (8)

(Or)

(b) (i) What is the use of test bench in Verilog HDL? Explain with one example. (8)

(ii) Write the verilog code for D-Latch and D-flipflop. (8)

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Reg. No. : 1 3 1 5 1 4 4

K.S.R. COLLEGE OF ENGINEERING, TIRUCHENGODE – 637 215

(AUTONOMOUS)

Question Paper Code : 152156

B. E. / B.Tech. DEGREE END SEMESTER EXAMINATION, JUNE 2016

Sixth Semester

B.E. – ELECTRONICS AND COMMUNICATION ENGINEERING

12EC3604 – VLSI design

(Regulations 2012)

Time: Three hours **Maximum Marks: 100**

Answer ALL Questions

PART A — (10 x 2 = 20 Marks)

1. Define Photolithography.
2. Outline the chip design hierarchy.
3. What is meant by body effect in MOS transistors?
4. Define latch up.
5. Give the principle of operation of transmission gates.
6. List the advantages of using Pass transistor logic.
7. Recall the principle of operation of dynamic logic circuits.
8. Sketch the diagram of 6T SRAM Cell.
9. Categorize the two blocks in behavioral modeling.
10. Write the test bench for AND gate.

PART B — (5 x 16 = 80 Marks)

11. (a) (i) Discuss the steps of n - well CMOS fabrication process with suitable diagram. (8)

(ii) Explain the following terms with respect to latch up: (8)

(1) Physical origin

(2) Latch - up prevention

(Or)

(b) (i) Describe SCMOS design rule set with examples. (8)

(ii) Illustrate Submicron CMOS process. (8)

12. (a) (i) Explain the large signal MOSFET model. (8)

(ii) Elaborate on the simulation of a circuit using SPICE with suitable flowchart. (8)

(Or)

(b) Construct the voltage transfer characteristics of CMOS inverter and explain the five regions of operation. (16)

13. (a) (i) Construct an AOI CMOS equivalent for the sum - of products expression Y= ABC+DE+EFG. (8)

(ii) Describe the structure of a standard cell design. (8)

(Or)

(b) Elaborate on

(i) Cell hierarchy (8)

(ii) Cell Libraries (8)

14. (a) (i) Elucidate the problem of cascading in dynamic logic circuits. How can it be overcome? (8)

(ii) Explain the working of a dynamic D Flip flop. (8)

(Or)

(b) (i) Compare static and dynamic CMOS logic Circuits. (8)

(ii) Explain the operation of Clocked CMOS logic circuit. (8)

15. (a) Explain the following with a suitable example.

(i) Timing Controls and Conditional Statements in Verilog. (8)

(ii) Behavior and Structural modeling in Verilog. (8)

(Or)

(b) (i) Develop the logic diagram of 4 to 1 MUX using NAND gates and write the gate level modeling using verilog HDL. (8)

(ii) Elaborate on the looping statements available in verilog HDL and write the verilog code for D - Latch. (8)

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Reg. No. : 1 2 1 5 0 1 2

K.S.R. COLLEGE OF ENGINEERING, TIRUCHENGODE – 637 215

(AUTONOMOUS)

Question Paper Code : 151145

B. E. / B.Tech. DEGREE END SEMESTER EXAMINATION, DEC 2015 / JAN 2016

Sixth Semester

B.E. – ELECTRONICS AND COMMUNICATION ENGINEERING

12EC3604 – VLSI Design

(Regulations 2012)

Time: Three hours Maximum Marks: 100

Answer ALL Questions

PART A — (10 x 2 = 20 Marks)

1. List the types of layout design rules.
2. What are the advantages of Twin-tub process?
3. Define Threshold voltage in CMOS.
4. Draw square law model of MOSFET.
5. Distinguish transmission gate and pass transistor.
6. Draw CMOS NAND gate.
7. List the gates in cell library.
8. What is the meant by latch up?
9. What are gate primitives? Give examples.
10. What are procedural assignments in verilog?

1 151145

PART B — (5 x 16 = 80 Marks)

11. (a) (i) Elaborate in detail about SOI CMOS Process. (10)

(ii) Explain about Chip Design Hierarchy with neat diagrams. (6)

(Or)

(b) (i) Describe in detail the SCMOS design rule set. (10)

(ii) Summarize briefly about construction of NMOS transistor. (6)

12. (a) (i) Detail about the techniques for latch up prevention. (8)

(ii) Discuss in detail the MOSFET Parasitic Capacitors and Resistors. (8)

(Or)

(b) (i) Elaborate the CMOS inverter DC characteristics with relevant equations. (10)

(ii) Write short notes on body effect. (6)

13. (a) (i) Draw the implementation of following complex logic expression using CMOS gates $Y = \overline{(A+B+C) \bullet D}$ (8)

(ii) Implement and explain tristate inverter using CMOS. (8)

(Or)

(b) (i) Construct the 2*1 Multiplexer & EXOR using transmission Gate. (10)

(ii) Write short notes on floor planning. (6)

14. (a) (i) Describe the operation domino logic circuit. (8)

(ii) Construct static RAM cell and explain it. (8)

(Or)

(b) Describe in detail dynamic logic circuit, and mention its advantages and disadvantages. Construct also dynamic DFF. (16)

15. (a) (i) Give the verilog code for full adder. Using it to implement 4 bit ripple carry adder. (10)

(ii) Briefly discuss about verilog operators. (6)

(Or)

(b) (i) Enumerate with an example bevioural modeling in verilog. (10)

(ii) Write a verilog code for priority encoder. (6)

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Reg. No. : 1 2 1 5 1 1 2

K.S.R. COLLEGE OF ENGINEERING, TIRUCHENGODE – 637 215

(AUTONOMOUS)

Question Paper Code : X6121

B. E. / B.Tech. DEGREE END SEMESTER EXAMINATION, JUNE 2015

Sixth Semester

B.E. – ELECTRONICS AND COMMUNICATION ENGINEERING

12EC3604 – VLSI Design

(Regulations 2012)

Time: Three hours **Maximum Marks: 100**

Answer ALL Questions

PART A — (10 x 2 = 20 Marks)

1. State Moore's law.
2. Mention the advantage of SOI process.
3. What is body effect?
4. Mention the significance of beta ratio of CMOS inverter.
5. List the various forms of CMOS logic structures.
6. Draw the CMOS realization of two input NAND gate.
7. Sketch the NOR based SR latch.
8. What is hold time of dynamic memories?
9. Mention the various operators in verilog.
10. Write the verilog module for half adder.

PART B — (5 x 16 = 80 Marks)

11. (a) (i) Explain in detail about P- well CMOS fabrication process with suitable sketches. (12)

(ii) Briefly discuss the photolithography process. (4)

(Or)

(b) (i) Discuss the SCMOS design layout rules. (12)

(ii) What is lambda based design rule? (4)

12. (a) (i) Derive the Ids Versus Vds relationship for a MOS transistor in all three regions of operation and draw the MOS transistor characteristics. (10)

(ii) Discuss the MOSFET capacitance model. (6)

(Or)

(b) (i) Explain the DC characteristics and transient characteristics of a CMOS inverter in different operating regions. (10)

(ii) Explain latch up in CMOS transistor. How it can be prevented? (6)

13. (a) (i) Discuss the method of obtaining the physical layout of CMOS NOR gate. (10)

(ii) Explain the operation of tristate inverter? (6)

(Or)

(b) (i) What is transmission gate? Design a 2 to 1 MUX using transmission gate. (8)

(ii) Briefly discuss pass transistor logic. (8)

14. (a) (i) Explain the operation of master slave D - flipflop. (8)

(ii) Draw the architecture of dynamic D - flipflop and explain. (8)

(Or)

(b) (i) Discuss the operation of 6 - transistor SRAM with neat sketch. (8)

(ii) Design two input AND gate using DOMINO logic. Also explain how domino logic is cascaded with different function. (8)

15. (a) (i) Explain the various operators used in verilog programming. (8)

(ii) Write the verilog coding for 3 to 8 decoder in behavior modeling. (8)

(Or)

(b) (i) What is test bench and explain with one example. (8)

(ii) Write the verilog code for full adder and 4 to 1 mux in gate level modeling. (8)

****