K.S.R. COLLEGE OF ENGINEERING: TIRUCHENGODE – 637 215.
(AUTONOMOUS)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
COURSE / LESSON PLAN SCHEDULE
16EC414 - MICROPROCESSORS AND MICROCONTROLLERS

NAME: Mr.R.VEERAMANI **CLASS: B.E/ II-ECE-A,B**

A). TEXT BOOKS:

1. N.Senthil Kumar, M.Saravanan, S.Jeevananthan, S.K.Shah, "Microprocessors and Interfacing 8086, 8051, 8096, and advanced processors", Oxford University Press, 2012
2. Krishna Kant, "Microprocessors and Microcontrollers Architecture, Programming and System Design Using 8085, 8086, 8051 And 8096", PHI 2014.

B). REFERENCES:

1. Muhammad Ali Mazidi, Janice Gillispie Mazidi, Rolin D.MCKinlay The 8051 Microcontroller and Embedded Systems, Second Edition, Pearson Education 2008.
2. Mohamed Rafiquzzaman "Microprocessor and Microcomputer Based System Design", 2nd Edition, CRC Press 1995.
3. Ramesh S Goankar – "Microprocessor Architecture Programming and Application with 8085" – penram Publications pvt – 5 E/Pearson 2000.
4. A K Ray, K M Bhurchandi, Advanced Microprocessors and Peripherals, TMH, 2007.
5. Douglas V Hall, "Microprocessors and Interfacing, Programming and Hardware" TMH, 2006.

C). LEGEND:

L	- Lecture	PPT	- Power Point
Tx	- Text	BB	- Black Board
OHP	- Over Head Projector	pp	- Pages
Rx	- Reference	Ex	- Extra

S.No.	Lecture Hour	Topics to be covered	Teaching Aid Required	Book No. / Page No.
UNIT – I 8 BIT MICROPROCESSOR ARCHITECTURE AND PROGRAMMING				
1.	L 1	Evolution, Introduction to Microprocessor	BB	Tx1/pp 14-16, Tx2/pp 34, Rx2/pp 73-75
2.	L 2	Address Bus, Data Bus and Control Bus	BB	Tx1/pp 19-22, Tx2/pp 35-36, Rx4/pp16-17
3.	L 3	Clock Generation	BB	Tx2/pp 37-38
4.	L 4	8085 – Hardware Architecture	BB+PPT	Tx1/pp 16-23,Tx2/pp 75-78, Rx2/pp 73-75 Rx3/pp 26-32
5.	L 5	Addressing Modes	BB	Tx1/pp 28-30, Tx2/pp 101-104, Rx2/pp 78-79
6.	L6	Instruction Set	BB+PPT	Tx1/pp 30-40, Tx2/pp 104-127,Rx2/pp 79-112, Rx3/pp 162-195
7.	L 7	Timing Diagrams	BB	Tx2/pp 89-96, Rx2/pp 112-115
8.	L 8	Interrupts	BB	Tx1/pp 21, Tx2/pp 82-85, Rx2/pp 141-153
9.	L9	Assembly Language Programming **Direct Memory Access timing diagram**	BB	Tx1/pp 40-41,Tx2/pp 107-108, 111-112, 116, 93-95, Rx2/pp 196-201
UNIT – II 16 BIT MICROPROCESSOR ARCHITECTURE AND PROGRAMMING				
10.	L 10	8086 – Hardware Architecture	BB+PPT	Tx1/pp 63-67, Tx2/pp 129-139, Rx2/pp 170-176, Rx3/pp 3-7, Rx5/pp 28-32
11.	L 11	Signals	BB	Tx1/pp 140-144

12.	L 12	Addressing Modes	BB	Tx1/pp 80-86, Tx2/pp 202-217, Rx2/pp 176-185
13.	L 13	Maximum mode and minimum mode configurations	BB	Tx1/pp 183
14.	L14	Assembler Directives	BB	Tx1/pp 217-222
15.	L 15	Instruction Set	BB	Tx1/pp 103-110, Tx2/pp 264-282, Rx2/pp 299-304
16.	L 16	Timing Diagram	BB	Tx2/pp 150-153, Rx5/pp 164-168
17.	L 17	Interrupts	BB	Tx1/pp 175-189, Tx2/pp 183-191, Rx2/pp 255-262 Rx4/pp 16-28
18.	L18	Assembly Language Programming**, Microprocessor with memory management and production**	BB+OHP	Tx1/pp 110-129, Tx2/pp 235-240, 250-252, 261-263, 276-281 Rx5/pp 543-547, Rx4/pp 444-502
UNIT – III MICROPROCESSOR PERIPHERAL INTERFACING				
19.	L19	Introduction to Interfacing	BB	Tx1/pp 391-392, Tx2/pp 480, Rx1/pp 19-26
20.	L20	8251 Serial Communication Interface	BB	**Tx1/pp**
21.	L21	Programmable Peripheral Interface (PPI)-Intel 8255	BB+PPT	Tx1/pp 240-249, Tx2/pp 301-311, Rx2/pp 170-176
22.	L22	Keyboard and Display Interface (8279)	BB+PPT	Tx1/pp 278-295, Tx2/pp 317-367, Rx2/pp 845-859 Rx4/pp 266-275
23.	L23	Programmable Interval timers (Intel 8253, 8254)	BB+PPT	Tx1/pp 295-307, Tx2/pp 367-397, Rx4/pp 235-248
24.	L24	8259 Interrupt Controller	BB	**Tx1/pp**
25.	L25	A-to-D converter	BB	Tx1/pp 259-263, Tx2/pp 407-419, Rx5/pp 304-306, Rx3 /pp212-223
26.	L26	D-to-A converter	BB	Tx1/pp 263-268, Tx2/pp 39-407, Rx5/pp 301-304, Rx4/pp 224-227
27.	L27	Printer Interface **Coprocessors**	BB	Tx1/pp 487-489, Tx2/pp 422-427, Rx2/pp 884-886
UNIT – IV 8 BIT MICROCONTROLLER ARCHITECTERES AND PROGRAMMING				
28.	L 28	8051 Microcontrollers – Hardware Architecture	BB+PPT	Tx1/pp 392-394,Tx2/pp 481-492, Rx4/pp 649-652
29.	L 29	SFR Special Function Register,	BB	Tx2/pp 486-489
30.	L 30	Input/output pins, External Memory	BB	Tx1/pp 426-437,Tx2/pp 501-505, Rx1/pp 75-87
31.	L 31	Counters and Timers	BB+OHP	Tx1/pp 437-445,Tx2/pp 528- 533, Rx1/pp201-231
32.	L 32	Serial Data Input/output	BB	Tx1/pp 533-547
33.	L 33	Interrupts, 8051 Addressing Modes	BB	Tx1/pp 445-450, 402-404, Tx2/pp 548-553, 571-576 Rx1/pp 271-290, Rx4/pp 661-665
34.	L 34	Arithmetic Instructions, Logical Instructions, Single bit Instructions	BB	Tx1/pp 404-410,Tx2/pp 577-605, Rx1/pp 115-147
35.	L 35, 36	Assembly Language Programming **RTC interface with 8051 microcontroller**	BB	Tx1/pp 410-426, 505-512,Tx2/pp 581-582, 587-588, 593-596, 602-605, Rx1 /pp 29-54,407-417
UNIT – V APPLICATIONS OF MICROPROCESSORS & MICROCONTROLLERS				
36.	L 37	8051 - Interfacing DC Motor	BB	Tx1/pp 487-489,Rx1/pp 441-450
37.	L 38	Stepper Motor	BB	Tx1/pp 268-273,Rx1/pp 432-440, Rx5/pp 281-283

38.	L 39,	Sensor interfacing	BB	Rx2/pp 348-352
39.	L 40	Relays	BB	Rx1 /pp 256-258
40.	L 41	Seven Segment Displays	BB	Rx1/pp 325-326
41.	L 42	Key Board	BB	Rx1/pp 311-317
42.	L 43	Realtime Clock	BB	Tx1/pp 487-489,Rx1/pp 441-450
43.	L 44	8051 - Interfacing LCD	BB+OHP	Tx1/pp 482-486,Rx1/pp 299-317
44.	L 45	Traffic Light Control	BB+OHP	Tx1/pp 256-259,Tx2/pp 644-682

UNIT – I 8 BIT MICROPROCESSOR ARCHITECTURE AND PROGRAMMING

1. **What is Microprocessor? (Remembering) (CO1)**

   It is a program controlled semiconductor device (IC}, which fetches, decode and executes instructions.

2. **Define microcomputer. (Remembering) (CO1)**

   A computer that is designed using a microprocessor as its CPU. It includes microprocessor, memory, and I/O.

3. **Summarize the basic units of a microprocessor. (Understanding) (CO1)**

   The basic units or blocks of a microprocessor are ALU, an array of registers and control unit.

4. **What is Software and Hardware?(Remembering) (CO1)**

   The Software is a set of instructions or commands needed for performing a specific task by a programmable device or a computing machine. The Hardware refers to the components or devices used to form computing machine in which the software can be run and tested. Without software the Hardware is an idle machine.

5. **Recall assembly language. (Remembering) (CO1)**

   The language in which the mnemonics (short -hand form of instructions) are used to write a program is called assembly language. The manufacturers of microprocessor give the mnemonics.

6. **Recall machine language. (Remembering) (CO1)**

   The software developed using 1's and 0′s are called machine language programs.

7. **Illustrate the drawback in machine language and assembly language programs. (Understanding) (CO1)**

   The machine language and assembly language programs are machine dependent. The programs developed using these languages for a particular machine cannot be directly run on another machine.

8. **Interpret opcode and operand. (Understanding) (CO1)**

   Opcode (Operation code) is the part of an instruction / directive that identifies a specific operation. Operand is a part of an instruction / directive that represents a value on which the instruction acts.

9. **Define mnemonics. (Remembering) (CO1)**

   The short-hand form of describing the instructions is called mnemonics. The mnemonics are given by the manufacturers of microprocessors.

10. **Define a program. (Remembering) (CO1)**

    A program is a sequence of instructions written to tell the computer to perform a specific function.

11. **Define bit, byte and word. (Remembering) (May-June 2010) (CO1)**

    A digit of the binary number or code is called bit. Also, the bit is the fundamental storage unit of computer memory.

    The 8-bit (8-digit) binary number or code is called byte and 16-bit binary number or code is called word. (Some microprocessor manufactures refer the basic data size operated by the processor as word).

12. **Explain the clock generation of 8085 microprocessor. (Understanding) (CO1)**

    Early microprocessors needed clock input to be given externally (i.e.,) an extra generator clock chips was necessary. The clock generator chips have two pins between which a crystal or an RC circuit could be connected for the generation of frequency desired. Nowadays the clock generator chips is embedded in to the microprocessor itself. A crystal or RC network connected between the two pins(X1 & X2) of microprocessor.

13. **Recall the functions of bus. (Remembering) (CO1)**

    Bus is a group of conducting lines that carries data, address and control signals.

14. Why data bus is bi-directional? (Remembering) (CO1) (DEC 2018)

The microprocessor has to fetch (read) the data from memory or input device for processing and after processing, it has to store (write) the data to memory or output device. Hence the data bus is bi-directional.

15. Why address bus is unidirectional? (Remembering) (CO1)

The address is an identification number used by the microprocessor to identify or access a memory location or I / O device. It is an output signal from the processor. Hence the address bus is unidirectional.

16. What do you mean by address bus? (Remembering) (CO1)

The address bus is a group of 16 lines generally identified as A0 to A15. The address bus is unidirectional: bits flow from MPU to peripheral devices.

17. What is the size of the address bus and data bus in a 8085 microprocessor? (Remembering) (DEC 2014) (CO1)

The size of the address bus and data bus of the 8085 microprocessor are 16 – bit and 8 – bit respectively.

18. Define control bus. (Remembering) (CO1)

This is single line that is generated by the MPU to provide timing and control signals of various operations.

19. Why are the program counter and the stack pointer 16-bit registers? (Remembering) (CO1)

Memory locations for the program counter and stack pointer have 16-bit addresses. So the PC and SP have 16-bit registers.

20. Illustrate the function of ALE and IO/M signals in the 8085 architecture. (Understanding) (CO1)

The ALE signal goes high at the beginning of each machine cycle indicating the availability of the address on the address bus, and the signal is used to latch the low order address bus. The IO/M signal is a status signal indicating whether the machine cycle is I/O or memory operation. The IO/M signal is combined with the RD and WR control signals to generate IOR, IOW, MEMW, MEMR.

21. What is an instruction? (Remembering) (CO1)

An instruction is a binary pattern entered through an input device in memory to command the microprocessor to perform specific function.

22. List out four primary operations of a MPU. (Understanding) (CO1)

1. Memory read 2. Memory write 3. I/O read 4. I/O write

23. What is the difference between CPU bus and system bus? (Remembering) (CO1)

The CPU bus has multiplexed lines but the system bus has separate lines for each signal. (The multiplexed CPU lines are demultiplexed by the CPU interface circuit to form system bus).

24. Interpret the need of system clock and how it is generated in 8085. (Understanding) (CO1)

The system clock is necessary for synchronizing various internal operations or devices in the microprocessor and to synchronize the microprocessor with other peripherals in the system.

25. What is multiplexing and what is its advantage? How the address and data lines are demultiplexed in 8085? (Remembering) (CO1)

Multiplexing is transferring different information at different well defined times through same lines. A group of such lines is called multiplexed bus. The advantage of multiplexing is that fewer pins are required for microprocessors to communicate with outside world. The low order address and data lines of 8085 are demultiplexed using an external 8-bit D-Latch (74LS373) and the ALE signal of 8085. Demultiplexing of address and data lines in 8085 processor At the beginning of every machine cycle, ALE is asserted high and then low. Also the low byte of address is given out through ADo - AD7 lines. Since the ALE is connected to Enable of Latch, when ALE is asserted high and then low the addresses are latched into the output lines of the latch. Now the lines ADo -AD7 are free for data transfer.

26. Illustrate the function of IO/M, READY , HOLD and HLDA in 8085. (Understanding) (CO1)

1. The IO/M is used to differentiate memory access and I/O access. For IN and OUT instruction it is high. For memory reference instructions it is low.
2. READY is an input signal to the processor, used by the memory or I/O devices to get extra time for data transfer or to introduce wait states in the bus cycles.
3. HOLD and HLDA signals are used for the Direct Memory Access (DMA) type of data transfer. The DMA controller place a high on HOLD pin in order to take control of the

system bus. The HOLD request is acknowledged by the 8085 by driving all its tristated pins to high impedance state and asserting HLDA signal high.

27. Recall the functions of an accumulator. (Remembering) (CO1) (JUNE 2014, Jan 2017)

An accumulator is an 8 bit 'A' Register. It is used to store the final results after execution of arithmetic and logical operations.

28. List the allowed register pair of 8085. (Remembering) (CO1) (JUNE 2014)

BC, DE, HL are the three allowed register pair of 8085.

29. What are the general purpose registers used in 8085? (Remembering) (CO1) (Nov-Dec2010, Jan 2016)

B, C, D, E, H & L - To store the 8-bit data.BC, DE & HL-Register pairs used to perform 16 bit operations.

30. Mention the Flag registers used in 8085. (Remembering) (CO1) (Nov-Dec2010)

Zero, carry, sign, parity and auxiliary flags.

31. What is a flag? List the flags of 8085. (Remembering) (CO1) (JUNE 2014)

Flag is a flip flop used to store the information about the status of the processor and the status of the instruction executed most recently. There are five flags in 8085. They are sign flag, zero flag, Auxiliary carry flag, parity flag and carry flag.

32. What is bus cycle? (Remembering) (CO1)

The bus cycle is the basic external operation performed by the processor. It is also known as processor cycle or machine cycle. To execute an instruction, the processor will run one or more bus cycles in a particular order.

33. What is T -state? (Remembering) (CO1) (May-June 2010)

The T-state is the time period of the internal clock signal of the processor. The time taken by the processor to execute the machine cycle is expressed in T-state.

34. What is processor cycle (Machine cycle), Instruction cycle, fetch and execute cycle? (Understanding) (CO1) (May-June 2010,2016)

The processor cycle or machine cycle is the basic operation performed by the processor. To execute an instruction, the processor will run one or more machine cycles in a particular order. The sequence of operations that a processor has to carry out, while executing the instruction is called Instruction cycle. Each instruction cycle of a processor in tum consists of a number of machine cycles. In general, the instruction cycle of an instruction can be divided into fetch and execute cycles. The fetch cycle is executed to fetch the opcode from memory. The execute cycle is executed to decode the instruction and to perform the work instructed by the instruction.

35. List the various machine cycles of 8085. (Remembering) (CO1)

The various machine cycles of8085 are

(i) Opcode fetch cycle (ii) Memory read cycle (iii) Memory write cycle

(iv) I/0 read cycle (v) I/0 write cycle (vi) Interrupt acknowledge cycle(vii) Bus idle cycle.

36. What is the need for timing diagram? (Remembering) (CO1)

The timing diagram provides information regarding the status of various signals, when a machine cycle is executed. The knowledge of timing diagram is essential for system designer to select matched peripheral devices like memories, latches, ports, etc., to form a microprocessor system.

37. What is addressing mode? What are the various addressing modes available in 8085? (Remembering) (CO1) DEC 2018

The method of specifying the data to be operated by the instruction is called addressing. The 8085 has the following five different types of addressing.

1. Immediate addressing 2. Direct addressing 3. Register addressing 4. Register indirect addressing

5. Implied addressing

38. What is an Interrupt? How the interrupt are classified? (Remembering) (CO1)(June2018)

Interrupt is a signal send by an external device to the processor so as to request the processor to perform a particular task or work. They are three methods of classifying interrupts.

Method I :The interrupts are classified into Hardware and Software interrupts

Method II: The interrupts are classified into vectored and Non- Vectored interrupt

39. What is vectored and Non- Vectored interrupt? (Remembering) (CO1)

When an interrupt is accepted, if the processor control branches to a specific address defined by the manufacturer then the interrupt is called vectored interrupt. In Non-vectored interrupt there is no specific address for storing the interrupt service routine. Hence the interrupted device should give the address of the ISR.

40. List the Software and Hardware interrupts of 8085. (Remembering) (CO1) (DEC 2014, Jan 2016, Jan 2017)

Software interrupts : RST 0, RSTl, RST 2,RST 3, RST 4, RST 5,RST 5.5,RST 6 and RST 7.

Hardware interrupts TRAP, INTR

41. Write about priority of interrupts. (Remembering) (CO1) (JUN 2015)

Priority order is : TRAP, RST 7.5, RST6.5 , RST 5.5 , INTR (Highest to Lowest)

42. Write 8085 assembly language instructions to store the contents of the flag register in memory location 2000H. (Creating)

```
PUSH PSW
POP B
MOV A, C
STA 2000H
HLT
```

43. Write an 8085 program to generate a time delay of 0.4sec given crystal frequency 5MHZ. (Creating) (CO1)

Operating frequency = 5/2 = 2.5MHZ.

Time for one T-state = 1/ 2.5MHZ = 0.4μsec.

Number of T-states required = Required Time/Time for 1T-state= 0.4sec/ 0.4μsec= 1M

Delay program:

```
LXI B,COUNT
Loop : DCX B
MOV A,C
ORA B
JNZ Loop
```

= 1 x 106 = 10 + (count – 1) x24 +21

count = 4166610

= A2C2H.

44. What is masking and why it is required? (Remembering) (CO1)

Masking is preventing the interrupt from disturbing the current program execution. When the processor is performing an important job (process) and if the process should not be interrupted then all the interrupts should be masked or disabled. In processor with multiple 'interrupts, the lower priority interrupt can be masked so as to prevent it from interrupting, the execution of interrupt service routine of higher priority interrupt.

45. When the 8085 processor accept hardware interrupt?(Analyzing) (CO1)

The processor keeps on checking the interrupt pins at the second T -state of last Machine cycle of every instruction. If the processor finds a valid interrupt signal and if the interrupt is unmasked and enabled then the processor accepts the interrupt. The acceptance of the interrupt is acknowledged by sending an OOA signal to the interrupted device.

46. When the 8085 processor will disable the interrupt system? (Analyzing) (CO1)

The interrupts of 8085 except TRAP are disabled after anyone of the following operations

1. Executing El instruction. 2. System or processor reset.
3. After reorganization (acceptance) of an interrupt.

47. How clock signals are generated in 8085 and what is the frequency of the internal clock? (Remembering) (CO1)

The 8085 has the clock generation circuit on the chip but an external quartz crystal or L C circuit or RC circuit should be connected at the pins XI and X2. The maximum internal clock frequency of 8085A is 3.03 MHz.

48. How many memory locations can be addressed by a microprocessor with 14 address lines? (Understanding) (CO1)

The 8085 MPU with its 14-bit address is capable of addressing 2^{14} =16,384 (ie) 16K memory locations.

49. If the 8085 adds 87H and 79H, specify the contents of the accumulator and the status of the S, Z, and CY flag. (Analyzing) (CO1)

The sum of 87H and 79H =100H. Therefore, the accumulator will have 00H, and the flags will be S =0, Z = 1, CY = 1

50. Write down the control and status signals. (Remembering) (CO1)

Two Control signals and three status signals:

Control signals: RD and WR, **Status signals**: IO/M, S1, S2

51. Define the types of branching operations. **(Remembering) (CO1)**

Jump: to test the conditions : Call, Return, And Restart: Change the sequence of the program

52. Define two-byte instruction with one example. (Remembering) (CO1)

In a 2-byte instruction, the first byte specifies the Opcode; the second byte specifies the operand. Example: Opcode operand binary code hex code MVI A, DATA - 0011 1110 3E First byte, DATA Data second byte

53. Write instructions to load the hexadecimal numbers 65H in register C, and 92h in the accumulator A. Display the number 65H at PORT0 and 92H at PORT1. (Creating) (CO1)

```
MVI C, 65H
MVI A, 92H
OUT PORT1 ; DISPLAY 92H
MOV A, C ; COPY C INTO A FOR DISPLAY
OUT PORT0 ; DISPLAY 65H
HLT
```

54. What operation can be performed by using the instruction ADD A? (Remembering) (CO1)

The instruction ADD a will add the content of the accumulator to itself; this is equivalent to multiplying by 2.

55. What operation can be performed by using the instruction SUB A? Specify the status of Z and CY? **(Remembering) (CO1)**

The instruction SUB a will clear the accumulator. The flag status will be CY = 0 and Z = 1.

56. Write instructions to a) load 00H to accumulator b) Decrement the accumulator c) Display the answer. (Remembering) (CO1)

```
MVI A, 00H (A = 0 0 0 0 0 0 0 0
DCR A - 0 0 0 0 0 0 0 1
OUT PORT# 1 1 1 1 1 1 1 1 = FFH
HLT
```

57. How is the instruction set classified based on their word size? (Remembering) (CO1)

The instruction set is classified in three groups according to the word size: 1-byte instruction, 2-byte instruction, 3-byte instruction

58. Recall the function of JNC 16-bit address. (Remembering) (CO1)

It changes the program sequence to the location specified by the 16-bit address if the carry flag is reset.

59. Give the instructions that perform the logical operations. (Remembering) (CO1)

AND, OR, Exclusive-OR, Rotate, Compare, Complement.

60. What is STA in data transfer instruction? (Remembering) (CO1)

Copy the data from the accumulator in the memory location specified by the 16-bit address

61. Give the difference between JZ and JNZ? (Remembering)

JZ change the program sequence to the location specified by the 16-bit address if the zero flag is set. **JNZ** change the program sequence to the location specified by the 16-bit address if the zero flag is reset.

62. What is the function of microprocessor in a system? (Remembering) (CO1)

The microprocessor is the master in the system, which controls all the activity of the system. It issues address and control signals and fetches the instruction and data from memory. Then it executes the instruction to take appropriate action.

63. Define stack and explain stack related instructions. (Remembering) (CO1)

The stack is a group of memory locations in the R/W memory that is used for the temporary storage of binary information during the execution of the program. The stack related instructions are PUSH & POP

64. How does the microprocessor differentiate between data and instruction(Understanding) (CO1)

When the first m/c code of an instruction is fetched and decoded in the instruction register, the microprocessor recognizes the number of bytes required to fetch the entire instruction. For example MVI A, Data, the second byte is always considered as data. If the data byte is omitted by mistake whatever is in that memory location will be considered as data & the byte after the "data" will be treated as the next instruction.

65. What are the instructions used for data transfer in 8085 microprocessor? (Rem) (CO1) (Dec 2009).

MOV, LDA, STA, LHLD, SHLD, PUSH, POP etc.

66. What are steps involved to fetch a byte in 8085? (Understanding) (CO1)

- The PC places the 16-bit memory address on the address bus
- The control unit sends the control signal RD to enable the memory chip
- The byte from the memory location is placed on the data bus
- The byte is placed in the instruction decoder of the microprocessor and the task is carried out according to the instruction

67. Explain LDA, STA and DAA instructions. (Understanding) (CO1)

LDA copies the data byte into accumulator from the memory location specified by the 16-bit address. STA copies the data byte from the accumulator in the memory location specified by 16-bit address. DAA changes the contents of the accumulator from binary to 4-bit BCD digits.

68. How the vector address is generated for the INTR interrupt of 8085? (Rem) (CO1)

For the interrupt INTR, the interrupting device has to place either RST opcode or CALL opcode followed by l6-bit address. I~RST opcode is placed then the corresponding vector address is generated by the processor. In case of CALL opcode the given l6-bit address will be the vector address.

69. Mention the classifications of 8085 instruction set. (Remembering) (CO1) (Nov-Dec2010)

Data transfer operations, arithmetic operations, branching operations and machine control operations are the classifications of 8085 instruction set.

70. List out the limitations of 8085. (Remembering) (CO1) (Nov-Dec2010)

a. The low order address bus is multiplexed with the data bus. The buses need to be demultiplexed.

b. Appropriate control signals need to be generated to interface memory and I/O with the 8085.

71. Difference between shift and rotate instructions. (Remembering) (CO1) (Jun 2015)

In shift instruction, last bit will be discarded during rotation. But in the case of rotate instruction last bit (D7) will be transferred to first bit(D0). If it rotate is thru carry the last bit (D7) will be transferred to carry and the carry bit transferred to first bit (D0).

72. What are PUSH and POP instructions? (Remembering) (May-June 2010) (CO1)

Stack is a part of read/write memory that is used for temporary storage of binary information during the execution of a program. PUSH instruction is used to write the information on the stack.POP instruction is used to read the information from the stack.

E.g. Push rp (M) ← (rp) and (SP) ← (SP) - 2, POP rp (rp) ← (M) ← and (SP) (SP) + 2

PART-B (16 MARK QUESTIONS)

1. Explain the architecture of 8085 microprocessor with the help of a diagram. (Understanding) **(**CO1) (May-June 2010, Jan 2016, June 2016, Jan 2017, JUNE 2018)
2. Explain the 5 functional categories of the instruction set of 8085 with at least two examples each. (Understanding) (CO1) (Nov-Dec 2003,2004 ,Nov/Dec 2011, June 2014, Jun 2015,Jan 2017)
3. Describe the signals present in 8085.(Remembering) (CO1) (Jun 2015)
4. Explain the various addressing modes in 8085 with example.(Understanding) (CO1) (Jun 2015. DEC 2018))
5. Draw the timing diagram of opcode fetch machine cycle memory read cycle and I/O write cycle in 8085 and explain them.(Understanding) (CO1) (IT Apr/may 2005, Jan 2016, DEC 2018)
6. Explain with the help of a suitable diagram how the INTR pin can be used to interrupt the 8085 and how it responds to the signal. (Understanding) (CO1) (ECE Apr/may 2005).
7. Explain various interrupts of 8086? (Understanding) (CO1) (June 2014, June 2016)

8. Draw the timing diagram for the instruction MVI A, FF.(Understanding) (CO1) (Dec 2014)
9. Draw the timing diagram of memory read cycle of 8085 microprocessor and explain the activities of the bus in each T-state.(Understanding) (CO1) (Nov-Dec 2009).
10. a. Discuss in detail about timing diagram. (Understanding) (CO1) (May-June 2010)
    b. Draw the timing diagram for the execution of the instruction MOV A, B in 8085 processor and explain. (8) (Understanding) (CO1)(May-June 2010).
11. Draw the timing diagram for 8085 instruction STA "574A"H. (Understanding) (CO1) (Nov-Dec 2004, Jan 2017)
12. Write an assembly language program based on 8085 microprocessor to convert a given 8 bit binary to three unpacked digits of BCD.(Creating) (CO1) (April-May 2004, Jun 2015 Jan 2017)
13. Write a program to count from 0 to 9 and 9 to 0 continuously with 1.5 sec delay between each count and display the count at one of the output ports. Draw a flow chart and show its delay calculations. (Creating) (CO1) (April-May 2005)
14. Write an 8085 assembly language program to perform 32-bit binary addition. (Creating) (CO1) (Nov-Dec 2005)
15. Write an assembly language program using 8085 instructions to add two n –byte numbers stored at memory locations starting at 'X' and 'Y' respectively. Store the results at memory location starting from 'Z'. Draw the flow chart. (Creating) (CO1) (Apr/may 2005).
16. Write an assembly language program using 8085 instructions to sort an array in ascending order. (Creating) (CO1)
17. Write an assembly language program using 8085 instructions to find the smallest element in an array. (Creating) (CO1)
18. Write a program to add a series of 10 numbers stored from location 3000 H onwards.(Nov/Dec 2011, 2014) (Creating) (CO1)
19. What will be the value in accumulator for the given 8085 program given below? (Analyzing) (CO1) (Dec 2005)

```
MVI C, 7F
MVI B,3E
MOV A,B
RLC
RLC
ANI 7F
HLT
```

20. Write assembly language program to find factorial of a number. (Creating)(CO1) (June 2016)
21. Compile assembly language program to perform ab+ac, where a, b, and c are 8-bit binary numbers. Explain with algorithm and flowchart. (Creating) (CO1) (June 2016)

UNIT – II 16 BIT MICROPROCESSOR ARCHITECTURE AND PROGRAMMING

1. What are the segment register in 8086 CPU?(Remembering)(CO2)(May-June 2010, 2015, Nov/Dec 2011)

1) Extra segment 2) Stack segment 3) data segment 4) Code segment

2. Illustrate difference between segment register and general purpose register. (Understanding) (CO2)

The segment registers are used to store 16 – bit segment base address of the four memory segments. The general purpose registers are used as the source or destination register during data transfer and computation, as pointers to memory and counters.

3. What is the purpose of segment registers in 8086? (Remembering)(CO2)

There are 4 segment registers present in 8086. They are the **code segment** register gives the address of the current code segment. ie. It will points out where the instructions, to be executed, are stored in the memory.

The **data segment** register points out where the operands are stored in the memory.

The **stack segment** registers points out the address of the current stack, which is used to store the temporary results. If the amount of data used is more the **Extra segment** register points out where the large amount of data is stored in the memory.

4. Illustrate the functions of bus interface unit (BIU) in 8086? (Remembering)(CO2)

(a) Fetch instructions from memory.

(b) Fetch data from memory and I/O ports.
(c) Write data to memory and I/O ports.
(d) To communicate with outside world.
(e) Provide external bus operations and bus control signals.

5. What is the clock frequency of 8086, 8086-2 8086-4? (Remembering) (CO2)(June 2016)

Internal clock Frequency: 5 MHz 8MHz 4MHz
External Clock Frequency: 15MHZ 24MHZ 12MHZ

6. List out the two modes of operations present in 8086. (Remembering)(CO2)

i. Minimum mode(or)Uniprocessor system ii) Maximum mode(or)Multiprocessor system

7. What is the maximum memory size that can be addressed by 8086? (Remembering)(CO2) (JUNE 2014)

The total number of address lines in 8086 is 20. So the maximum memory size addressed by the 8086 microprocessor is 1MB.

8. What is instruction queue? Explain its advantages. (or) How the speed is increased in 8086 microprocessor? (Remembering) (CO2)(DEC 2014)

To speed up the program execution, the BIU fetches si x instruction bytes ahead of time from the memory. These prefetched instruction bytes are held for the execution unit in a group of registers called queue. With the help of queue it is possible to fetch next instruction when current instruction is in execution.

9. Define pipelining. (Remembering) (CO2)(May / June 2013, 2015,2016)

Feature of fetching the next instruction while the current instruction is executing is called pipelining.

10. How physical address is generated in 8086? (Understanding)(CO2)

The content of the segment register are multiplied by 16 i.e., shifted by 4 position to the left by inserting 4 zero bits and then the offset i.e., the contents of IP register are added to the shifted contents of segment register to generate physical address.

11. The CS contains A280, while the IP contains CE24. Evaluate the resulting physical address. (Remembering) (CO2)(Jun 2015)

Content of Code Segment ----- $A280_h$
Content of Instruction Pointer ----- $CE24_h$

Left Shift the content of CS by 4 times or Multiply the CS content by 10_h. Then add that with the content of IP to get the physical address.

Content of Code Segment after shifting ----- $A2800_h$
Content of Instruction Pointer ----- $CE24_h$
The physical address obtained is ----- $AF64_h$

12. List the merits of memory segmentation. (Remembering)(CO2)

- It allows the memory addressing to be 1Mega Byte(MB) even though the address associated with individual instruction is only 16 bit.
- It allows instruction code, data, stack and portion of program to be more than 64KB long by using more than one code, data, stack segment and extra segment.
- It facilitates use of separate memory areas for program, data and stack.
- It permits a program or its to be put in different areas of memory, each time the program is executed i.e., program can be relocated which is very useful in multiprogramming.

13. What are control bits? (Remembering)(CO2)

The flags TF, IF and DF of 8086 are used to control the processor and so they are called control bits.

14. How many address lines and data lines available in 8086 CPU? (Remembering) (CO2)(May / Jun 2010) In 8086, an memory location is addressed by 20 bit address and the address bus is 20 bit address and the address bus is 20 bits. So it can address up to one mega byte (2^20) of memory space.

15. List the operating modes of 8086 and which pin decides the operating mode. (Remembering) (CO2)(May-June 2010).

Minimum mode and Maximum mode are the operating modes of 8086.Pin MIN/MAX pin decide the operating mode.

16. List out the functions of the pointers SP and BP in 8086? (Remembering)(CO2)(May 2010).

SP (Stack Pointer): It contains the 16-bit offset from the start of the segment to the top of stack. It is used for stack operation. For stack operation, physical address is produced by adding the contents of stack pointer register to the segment base address.

BP (Base pointer): Base pointer is used instead of SP for accessing the stack using the based addressing mode. In this case, the 20-bit physical address is calculated from BP and SS.

17. What do you mean by index register? (Remembering) (CO2)

The index register DI and SI are used as a general purpose registers as well as for offset storage in case of indexed and relative based addressing modes.

18. What are the functions of SI and DI registers? (Remembering) (CO2) (April-May 2005)

Source index (SI) can be used to hold the offset of a data word in the data segment. In this case, the 20-bit physical data address is calculated from Si and DS.

Destination Index (DI): The ES register points to the xetra segment in which data is stored. String instructions always use ES and DI to determine the 20 – bit physical address for the destination.

19. How do 8086 interrupts occur? (Analyzing) (CO2)

An 8086 interrupt can come from any of the following three sources

1) External signals 2.Special instructions in the program

3.Condition produced by instruction

20. What is interrupt acknowledge cycle? (Remembering) (CO2)

The interrupt acknowledge cycle is a bus cycle executed by 8086 processor after acceptance of an interrupt to get the interrupt type number or pointer, in order to service the interrupting device.

21. What are the 8086 interrupt types? Or What are the predefined interrupts in 8086? (Remembering) (CO2) (Nov/Dec 2011)

Dedicated interrupts

Type 0: Divide by zero interrupt
Type 1: Single step interrupt
Type 2:Non maskable interrupt
Type 3: Breakpoint
Type 4: Overflow interrupt
Type 0-255 Software interrupts

22. What is interrupt service routine? (Remembering) (CO2)

Interrupt means to break the sequence of operation. While the CPU is executing a program an interrupt breaks the normal sequence of execution of instructions & diverts its execution to some other program. This program to which the control is transferred is called the interrupt service routine.

23. Illustrate the function of the signal BHE in 8086. (Understanding)(CO2)(Jun 2015)

BHE signal means Bus High Enable signal. The BHE signal is made low when there is some read or write operation is carried out. ie . Whenever the data bus of the system is busy i.e. whenever there is some data transfer then the BHE signal is made low.

24. List out the different flag available in status register of 8086. (Remembering) (CO2) (June 2014, Jan 2017)

There are 6 one bit flags are present. They are,

AF - Auxiliary Carry Flag, CF - Carry Flag, OF - Overflow Flag, SF - Sign Flag

PF - Parity Flag, ZF - Zero Flag

25. How single stepping can be done in 8086? (Understanding) (CO2)

By setting the Trace Flag (TF) the 8086 goes to single-step mode. In this mode, after the execution of each instruction s 8086 generates an internal interrupt and by writing some interrupt service routine we can display the content of desired registers and memory locations. So it is useful for debugging the program.

26. State the significance of LOCK signal in 8086. (Understanding) (CO2)

If 8086 is working at maximum mode, there are multiprocessors are present. If the system bus is given to a processor then the LOCK signal is made low. That means the system bus is busy and it cannot be given of any other processors. After the use of the system bus again the LOCK signal is made high. That means it is ready to give the system bus to any processor.

27. What are the three classifications of 8086 interrupts? (Remembering) (CO2)

(1) Predefined interrupts (2) User defined Hardware interrupts (3) User defined software interrupts.

28. When the 8086 processor will enter wait state? (Understanding) (CO2)

The 8086 processor will check for READY signal at the second T-state of a bus cyle. If the READY is tied low at this time, then it will enter into wait state. (i.e., after second T-state). The processor will come out of wait state only when READY is again made high.

29. What happen in 8086 when DEN=0 and DIR=1? (Understanding) (CO2)

Informs the transceiver that CPU is ready for send and receive data.

30. What are the functions of status pins in 8086? (Remembering) (CO2)

S2	S1	S0
0	0	0 ---- Interrupt acknowledge
0	0	1 ---- Read I/O
0	1	0 ---- Write I/O
0	1	1 ---- Halt
1	0	0 ---- Code access
1	0	1 ---- Read memory
1	1	0 ---- Write memory
1	1	1 ---- inactive

S4	S3
0	0 --I/O from extra segment
0	1 --I/O from Stack Segment
1	0 --I/O from Code segment
1	1 --I/O from Data segment

S5 --Status of interrupt enable flag

S6 --Hold acknowledge for system bus

S7 --Address transfer.

31. What are the functions of BIU? (Remembering) (CO2) (Nov-Dec 2010)

BIU sends out addresses, fetches instructions from memory, reads data from ports and memory, and writes data to ports and memory.

32. What is Software interrupt? ((Remembering) (CO2)Nov-Dec 2010 June 2018)

Source of an interrupt is execution of the interrupt instruction.INT is referred as software interrupt.

33. List out the partitions of memory segments. (Remembering) (CO2) (Nov-Dec 2010)

Code segment, Stack segment, data segment and extra segment.

34. How the operating mode of 8086 is determined? (Remembering) (CO2) (Nov-Dec 2010)

By the logic level applied to the MN/MX input, pin 33 is high, 8086 functions in minimum mode and if low, 8086 functions in minimum mode.

35. How the clock signal is generated in 8086 microprocessor and what is the maximum internal clock frequency? (Understanding) (CO2) (Nov-Dec 2009).

8086 does not have an internal clock circuit.8284 clock generator is used to generate the required clock.8086 divides the clock signal supplied by the clock generator by three for internal clock requirement.

36. When the ready signal is sampled by the processor? (Understanding) (CO2) (Nov 2009).

The 8085 processor samples or checks the READY signal at the second T-State of every machine cycle.

37. What is masking of interrupts and why is it needed? (Remembering) (CO2) (Nov 2009).

Masking is preventing the interrupt from disturbing the current program execution. When the processor is performing an important job and if the process should not be interrupted then all the interrupts should be masked or disabled.

38. What is EU in 8086? (Remembering) (CO2) (May-June 2010).

EU is the Execution Unit in 8086 internal architecture. It tells the BIU from where to fetch instructions or data, decodes instructions and executes instructions.

39. What is the size of 8086 instruction? (Remembering) (CO2)

The size of 8086 instruction is one to six bytes. The first byte consists of opcode and special bit indicators. The second byte will specify the addressing mode of the operands. The subsequent bytes will specify immediate data or address.

40. What is addressing mode? How many addressing modes are there in 8086? (Rem) (CO2) (June 10, jan 2016, june 2018).

The 8086 has following 12 addressing modes.

1) Register addressing, Based index addressing, Immediate addressing, String addressing
2) Direct addressing, Direct I/O port addressing, Register addressing Indirect I/O port addressing
3) Based addressing, Relative I/O port addressing, Indexed addressing, Implied addressing

41. What is register addressing? (Remembering) (CO2) (Nov-Dec 2010)

In register addressing the instruction will specify the name of the register which holds the data to be operated by the instruction. Eg., MOV CX, DX.

42. What is immediate addressing? (Remembering) (CO2)

In immediate addressing mode an 8-bit or 16 bit data is specified as part of the instruction. Eg., MOV BX, 0CA5H.

43. What is Direct addressing in 8086? (Remembering) (CO2)

In direct addressing an unsigned 16-bit displacement or signed 8-bit displacement will be specified in the instruction. The displacement is the effective address of the data. The 20-bit physical address of the data is computed by multiplying the content of DS register by 16_{10} and adding to effective address. Eg., MOV CL, [0F2AH].

44. What is Register indirect addressing in 8086? (Remembering) (CO2)(DEC 2018)

In register indirect addressing the name of the register which holds effective address of data will be specified in the instruction. The register used to hold the effective addresses are BX, SI or DI. The 20-bit physical address of data is obtained by multiplying the content DS register by 16_{10} and adding to effective address. Eg., MOV DX, [DI].

45. What is based addressing in 8086? (Remembering) (CO2)

In based addressing the EA of data is specified as sum of base value and displacement. The register BX or BP is used to hold the data. When BX holds base value, the 20-bit physical address of data is calculated by multiplying the content of DS register by16_{10} and adding to effective address. When BP holds base value, it is calculated by multiplying the content of SS register by 16_{10} and adding to effective address. Eg., MOV CX,[BP + 002AH].

46. What is indexed addressing in 8086? (Remembering) (CO2)

In indexed addressing the EA of data is specified as a sum of index value and displacement. The register SI or DI is used to hold the index value. The 20-bit physical address of data is completed by multiplying the content of DS register by 16_{10} and adding to effective address. Eg., MOV AX, [DI + 04H].

47. What is based indexed addressing in 8086? (Remembering) (CO2)

In based indexed addressing the EA is specified as a sum of base value, index value and displacement. The base value is stored in BX or BP & the index value is stored in SI or Di register. When BX holds base value, the content of DS is considered as segment base address and when BP holds base value, the content of SS is considered as segment base address. Eg., MOV CX, [BP +DI +010AH].

48. How the 8086 instructions are classified? (Understanding) (CO2)

8086 instructions are classified as follows:

(i) Data transfer group (ii) arithmetic group (iii) Logical Group (iv) Control transfer group

(v) Miscellaneous Instruction group.

49. Mention the flag transfer instructions in 8086. (Remembering) (CO2) (Nov-Dec 2010)

LAHF, SAHF, PUSHF, POPF.

50. How the program execution transfer instructions are used in 8086? (Understanding) (CO2) (Nov-Dec 2010)

These instructions are used to tell the 8086 to the 8086 to start fetching instructions from some new address, rather than continuing in sequence.

51. What are the operations performed by string instructions in 8086 microprocessor? (Remembering) (CO2) (Nov-Dec 2009).

The operations performed by string instructions are, Repeat, Coping, Comparing, Loading and Storing. Example instructions: REP, MOVS, CMPS, LODS and STOS.

52. Give some examples of string instructions of 8086. (Understanding) (CO2) (May-June 2010, Jan 2017).

REP/REPE/REPZ/REPNE/REPNZ, MOVS/MOVSB/MOVSN, CMPS/CMPSB/CMPSW

53. Give the assembly language program statement format. (Remembering) (CO2) (Nov-Dec 2010)

LABEL FIELD	OPCODE FIELD	OPERAND FIELD	COMMENT FIELD
NEXT	ADD	AL, 07H	Add the contents

54. What is the difference between CALL and JUMP instruction? (Remembering) (CO2) (Nov-Dec 2009).

In CALL instruction, the address of next instruction is pushed to stack (i.e. stored in stack memory) before transferring the program control to call address. But in Jump instruction, the address of next instruction is not saved.

55. What is the operation carried out when 8086 executes the instruction MOVSW? (Remembering) (CO2)

Move string word: moves a string word ata time from source memory DS: SI to destination memory ES: Si & DI are incremented /decremented by 2 depending upon direction flag.

56. Name the external hardware synchronization instruction of 8086 processor.(Rem) (CO2)

1) HLT – Instruction 2) ESC- Instruction 3) LOCK- Instruction 4) NOP- Instruction
5) WAIT – Instruction

57. What is Segment override Prefix? Give example.(Remembering)(CO2)(June 2016)

It is the mechanism to allow the programmer to deviate from default segment and offset register mechanism. The segment override prefix is an additional byte that appears at the beginning of an instruction, to select alternative segment register.

PART – B (16 MARK QUESTIONS)

1. Discuss interrupts and interrupt routines. (Understanding)(CO2)(Nov-Dec 2003)
2. Explain all the pins of 8086. (Understanding) (CO2) (June 2014)
3. Explain the interrupt types available in 8086 with their priority levels and specify the action when an interrupt is executed. (Understanding) (CO2) (April-May 2004, May-June 2010, June 2014, Jan 2017)
4. Discuss the pipeline architecture 8086 and explain different addressing modes in 8086. (Understanding) (CO2) (Nov-Dec 2004,Dec 2011, June 2014, Jun 2015, Jan 2016, Jan 2017) (June 2018)
5. List out different types of addressing modes in 8086 and explain each mode with necessary examples. (Understanding) (CO2) (May-June 2010, Nov/Dec 2011, June 2014, Dec 2104, Jan 2016, June 2016, Dec 2018).
6. Explain memory organization of 8086. Bring out difference between 8086 and 8088. (Understanding) (CO2) (Nov-Dec 2004, 2010)
7. Explain briefly 8086 based MINIMUM mode and MAXIMUM mode CPU module with diagrams. (CO2) (Understanding) (CO2) (Apr-May2005, June 2016)
8. What are the control transfer instructions of 8086 microprocessor and explain. (Understanding) (CO2) (Nov-Dec 2009)
9. With the help of an example describe an action performed by 8086 for any two of the following instructions. (Applying) (CO2)(April-May 2005)
   a) AAM b) IMUL c) CMPSB d) ROL
10. Develop an ALP using 8086 to transfer a block of 20 data from one location of memory to another location. (Creating) (CO2)(EEE Apr-May 2005) (Nov/Dec 2011)
11. Explain various types of instructions used in 8086 with suitable examples. (Understanding) (CO2) (Nov-Dec 2010, Jun 2015, June 2018).
12. Develop an ALP to find the largest number in the series of signed numbers using 8086. (Creating)(CO2)(Nov/Dec 2011, Dec 2014, Jun 2015).
13. Develop an assembly program for sorting the array of bytes.(Creating)(CO2)
14. List and explain various arithmetic & logical instructions supported by 8086.(Remembering)(CO2)(Nov/Dec 2011)
15. Give examples for single operand instruction and double operand instruction in 8086. (Understanding) (CO2) (May-June 2010).
16. Explain the stack structure of 8086. Compile a simple program to illustrate the concept of programming the stack.(Understanding)(CO2) (June 2016)
17. Compare and contrast minimum and maximum mode operation of 8086. (June 2018)
18. Write an ALP for finding largest number. (June 2018)

UNIT III MICROPROCESSOR PERIPHERAL INTERFACING

1. Why interfacing needed for I/O devices? (Analyzing)(CO3)(Jun 2015)

Normally the speed of the processor is high when compared to the peripherals. So to cope up with the peripherals, processor has to wait for sometimes. Also the processor is able to perform

all the tasks of connecting I/O devices. But it should spend some time. So to reduce the burden of the processor interfacing is needed.

2. List the operating modes of 8255A PPI. (Remembering) (CO3)(JUNE 2014, Dec 2014)

Mode 0, Mode 1 and Mode 2

3. List the types of registers available in 8255A PPI. (Remembering) (CO3)

1. Two 8-bit ports (A and B) 2. Two 4-bit ports (Cu and CL)
3. Data bus buffer 4. Control logic

4. What is the purpose for the 8255 PPI? (Remembering) (CO3)

The 8255A is a widely used, programmable, parallel I/O device. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O.

5. Specify the bit of a control word for the 8255, which differentiates between the I/O mode and the BSR mode.(Understanding)(CO3)

BSR mode - D7= 0, and I/O mode - D7 = 1

6. Write the input/output feature in Mode 0 for the 8255A PPI. (Remembering) (CO3)

_ Outputs are latched
_ Inputs are not latched
_ Ports do not have handshake or interrupt capability

7. Write down the output control signals used in 8255A PPI? (Remembering) (CO3)

1. OBF _output Buffer Full 2. ACK _Acknowledge
3. INTR _Interrupt request 4. INTE _Interrupt Enable

8. What are the basic modes of operation of 8255? (Remembering) (CO3)(DEC 2018)

There are two basic modes of operation of 8255, viz.

1. I/O mode., 2. BSR mode. In I/O mode, the 8255 ports work as programmable I/O ports, while in BSR mode only port C (PC0-PC7) can be used to set or reset its individual port bits. Under the IO mode of operation, further there are three modes of operation of 8 255, So as to support different types of applications, viz. mode 0, mode 1 and mode 2.

Mode 0 - Basic I/O mode
Mode 1 - Strobed I/O mode , Mode 2 - Strobed bi-directional I/O

9. List out the features of mode 0 in 8255. (Remembering) (CO3)(DEC 2018)

1. Two 8-bit ports (port A and port B) and two 4-bit ports (port C upper and lower) are available. The two 4-bit ports can be combined used as a third 8-bit port.
2. Any port can be used as an input or output port.
3. Output ports are latched. Input ports are not latched.
4. A maximum of four ports are available so that overall 16 I/O configurations are possible.

10. What are the features used mode 1 in 8255? (Remembering) (CO3) (DEC 2018)

Two groups – group A and group B are available for strobed data transfer.

1. Each group contains one 8-bit data I/O port and one 4-bit control/data port.
2. The 8-bit data port can be either used as input or output port. The inputs and outputs both are latched.
3. Out of 8-bit port C, PC0-PC2 is used to generate control signals for port B and PC3=PC5 are used to generate control signals for port A. The lines PC6, PC7 may be used as independent data lines.

11. What are the signals used in input control signal & output control signal? (Remembering) (CO3)

Input control signal	**Output control signal**
STB (Strobe input)	OBF (Output buffer full)
IBF (Input buffer full)	ACK (Acknowledge input)
INTR(Interrupt request)	INTR(Interrupt request)

12. What are the features used mode 2 in 8255? (Remembering) (CO3)

The single 8-bit port in-group A is available.

1. The 8-bit port is bi-directional and additionally a 5-bit control port is available.
2. Three I/O lines are available at port C, viz PC2-PC0.
3. Inputs and outputs are both latched.
4. The 5-bit control port C (PC3=PC7) is used for generating/accepting handshake signals for the 8-bit data transfer on port A.

13. State the internal addresses for 8255A. (Remembering) (CO3) (Nov-Dec 2010)

Port A-00, Port B-01, Port C-10, Control-11.

14. **Mention the Programmable Peripheral Interface IC. What is the function of it? (Remembering) (CO3) (May-June 2010).**

8255-Programmable Peripheral Interface IC. The main function of it is to allow for parallel data transfer.

15. **List the major components of 8279 keyboard /display interface. (Remembering) (CO3)**

1. Keyboard section 2. Scan section
3. Display section 4. MPU interface

16. **What is the purpose for scan section in Keyboard interface? (Remembering) (CO3)**

The scan section has a scan counter and four scan lines. These scan lines can be decoded using a 4-to-16 decoder to generate 16 lines for scanning.

17. **List out the modes used in keyboard controller. (Remembering) (CO3)**

1. Scanned Keyboard mode with 2 Key Lockout.2. Scanned Keyboard with N-key Rollover.
3. Scanned Keyboard special Error Mode.4. Sensor Matrix Mode.

18. **What is the output modes used in 8279? (Remembering) (CO3) (JUNE 2014)**

8279 provides two output modes for selecting the display options.

1.Display Scan

In this mode, 8279 provides 8 or 16 character-multiplexed displays those can be organized as dual 4-bit or single 8-bit display units.

2.Display Entry

8279 allows options for data entry on the displays. The display data is entered for display from the right side or from the left side.

19. **What is the difference between 2 key locout and N key roll over modes in 8279? (Understandng) (CO3) (Nov/Dec 2011)**

Scanned Keyboard with N-Key Rollover :

In this mode, each key depression is treated independently. When a key is pressed, the debounce circuit waits for 2 keyboards scans and then checks whether the key is still depressed. If it is still depressed, the code is entered in FIFO RAM. Any number of keys can be pressed simultaneously and recognized in the order, the keyboard scan recorded them. All the codes of such keys are entered into FIFO. In this mode, the first pressed key need not be released before the second is pressed. All the keys are sensed in the order of their depression, rather in the order the keyboard scan senses them, and independent of the order of their release.

Scanned Keyboard mode with 2 Key Lockout :

In this mode of operation, when a key is pressed, a debounce logic comes into operation. During the next two scans, other keys are checked for closure and if no other key is pressed the first pressed key is identified. The key code of the identified key is entered into the FIFO with SHIFT and CNTL status, provided the FIFO is not full, i.e. it has at least one byte free. If the FIFO does not have any free byte, naturally the key data will not be entered and the error flag is set. If FIFO has at least one byte free, the above code is entered into it and the 8279 generates an interrupt on IRQ line to the CPU to inform about the previous key closures. If another key is found closed during the first key, the keycode is entered in FIFO. If the first pressed key is released before the others, the first will be ignored. A key code is entered to FIFO only once for each valid depression, independent of other keys pressed along with it, or released before it. If two keys are pressed within a debounce cycle (simultaneously), no key is recognized till one of them remains closed and the other is released. The last key, that remains depressed is considered as single valid key depression.

20. **List out the modes used in display modes. (Remembering) (CO3)**

1. Left Entry mode

In the left entry mode, the data is entered from the left side of the display unit.

2. Right Entry Mode

In the right entry mode, the first entry to be displayed is entered on the rightmost display.

21. **How the 8279 was initialized? (Understanding)(CO3)(Nov-Dec 2010)**

The first control word to initialize the 8279 is the Keyboard/display mode set word. The bits labeled DD in the control word specify whether the 8 digits or 16 digits to refresh.

22. **Define parallel-to-serial conversion. (Remembering) (CO3)**

In serial transmission, an 8-bit parallel word should be converted in to a stream of eight serial bits. This is known as parallel-to-serial conversion

23. Define serial-to-parallel conversion. (Remembering) (CO3)

In serial reception, the MPU receives a stream of eight bits and it is converted in to 8-bit parallel word. This is known as serial -to- parallel conversion.

24. Define Baud. (Remembering) (CO3)

The rate at which the bits are transmitted is called Baud.

25. Recall an instruction for serial output data? (Remembering) (CO3)

MVI A, 80H ;Set D7 in the accumulator = 1

RAR ;Set D6 = 1, SIM.

26. Illustrate the function of programmable interval timer chip. (US) (CO3) (Dec 2014)

The programmable interval timer chip is used to count the events, provide the required timing for the devices to operate and to generate certain amount of delay**.**

27. Write the steps necessary to initialize a counter in write operations.

1. Write a control word into the control registers

2. Load the low-order address byte 3. Load the high order byte

28. Give the various modes of 8254 timer. (Remembering) (CO3)

1. Mode 0: interrupt or terminal count 2. Mode 1: Rate generator

3. Mode 3:square wave generator 4. Mode 4: software triggered strobe

5. Mode 5:hardware triggered strobe

29. What is read back command in 8254 timer? (Remembering) (CO3)

The Read- Back Command in 8254 allows the user to read the count and the status of the counter.

30. What is the function of GATE signal in timer 8254? (Remembering) (CO3) (Nov-Dec 2009).

Gate Signal is used to enable or disable the counting process in 8254.GATE has no effect on OUT Signal. If Gate = 1 enables counting, Gate = 0, disables counting.

31. What are the operational modes of programmable timer IC? (Remembering) (CO3) (May-June 2010). Mode-0: Interrupt on Terminal count, Mode-1: Hardware Triggerable one-shot, Mode-2: Rate Generator, Mode-3: Square wave generator, Mode-4: Software Triggered Strobe and Mode 5: Hardware triggered strobe.

32. What is the maximum clock frequency and read-back feature of 8254? (Remembering) (CO3) (Nov-Dec 2010)

Maximum clock frequency is 8 Mhz and read-back feature is to latch the count in all the counters and the status of the counter at any point.

33. What are the different types of methods used for data transmission? (Remembering) (CO3)

The data transmission between two points involves unidirectional or bi-directional transmission of meaningful digital data through a medium. There are basically there modes of data transmission. (a) Simplex, (b) Duplex, (c) Half Duplex

34. What is synchronous data transfer? (Remembering) (CO3)

It is a data method which is used when the I/O device and the microprocessor match in speed. To transfer a data to or from the device, the user program issues a suitable instruction addressing the device. The data transfer is completed at the end of the execution of this instruction.

35. What is asynchronous data transfer? (Remembering) (CO3)

It is a data transfer method which is used when the speed of an I/O device does not match with the speed of the microprocessor. Asynchronous data transfer is also called as Handshaking.

36. What are the different types of write operations used in 8253? (Remembering) (CO3) (June 2016)

There are two types of write operations in 8253

(1) Writing a control word register (2) Writing a count value into a count register

37. Define scan counter. (Remembering) (CO3)

The scan counter has two modes to scan the key matrix and refresh the display. In the encoded mode, the counter provides binary count that is to be externally decoded to provide the scan lines for keyboard and display. In the decoded scan mode, the counter internally decodes the least significant 2 bits and provides a decoded 1 out of 4 scan on SL0-SL3.The keyboard and display both are in the same mode at a time.

38. What is resolution and conversion time in ADC? (Remembering) (CO3)

RESOLUTION TIME:

It is defined as the ratio of a change in value of input voltage Vi, needed to change the digital output by 1LSB. If the full scale input voltage required to cause a digital output of all 1's is Vifs.

CONVERSION TIME:

It is defined as the total time required to convert an analog signal into its digital output.

39. What is the significance of end of conversion signal while interfacing A/D converter to a microprocessor? (Remembering) (CO3)

The end of conversion signal indicates that the A/D conversion is completed so that microprocessor can read digital data from ADC.

40. Why ADC and DAC is used in microprocessor based system?(Analzing)(CO3)

More over the development in the microprocessor technology has made it compulsory to process data in the digital form. Since digital system such as microprocessor use a binary system of ones and zero, we have to convert signal from analog form to digital form. The circuits that performs this conversion is called ADC. On the other hand DACs are used when a binary output from a digital system must be converted to some equivalent analog voltage or current.

41. To which port of CPU, do we connect printer? (Understanding) (CO3)

In the parallel port of CPU the printer can be connected.

42. What are the control signals used in A/D converters? (Remembering) (CO3) Jan 2017.

Start of conversion signal (SOC) , End of Conversiom Signal (EOC), Output Enable (OE)

PART B: (16 MARK QUESTIONS)

1. Elaborate the functions of each block in the architecture of 8255 with necessary diagram.(Creating)(CO3) (June 2014, Jan 2017)
2. Explain in detail about any two operating modes of 8255 PPI. Show the control word format of 8255 and explain how each bit is programmed? (Understanding) (CO3) (Jan 2016 June 2016)
3. Discuss the features of Intel's programmable timer and explain its different modes of operation. (Creating)(CO3)(Nov-Dec2003,Nov / Dec 2009 2011, Dec 2014, Jun 2015, Jan 2016)
4. With block diagram describe the structure and operation of a keyboard / display controller. (Understanding)(CO3)(Nov-Dec2003, June 2014, Dec 2014, Jun 2015, June 2016, Jan 2017)
5. With a neat block diagram explain programmable interval timer.(Understanding)(CO3)
6. What is a Programmable Interval Timer (TIMER)? How is a 8254 used for generation of timing pulses output with its five different modes? (Understanding) (CO3) (Apr-May2004)(June 2018)
7. List the major components of the 8279 keyboard/display interface and explain their functions with neat diagram. (Understanding) (CO3) (Nov-Dec 2009).
8. Develop an ALP to generate triangular waveform using DAC0800. (Creating) (CO3)(Nov 2011)
9. Explain the printer interface in detail. (Understanding) (CO3)
10. Explain the DC motor interface with neat diagram. (Understanding) (CO3)
11. Briefly explain the method of interfacing A-D converter with microprocessor. (Understanding) (CO3) (Jun 2015).
12. Explain interfacing of D/A converter with microprocessor. (Understanding) (CO3) (June 2014)
13. Compile a program to generate a square wave of 1Hz frequency on OUT1 pin of 8253/54. Assume CLK1 frequency is 1Mhz and address for control register-0BH, counter1=09H, counter 2=0AH (Creating) (CO3)(June 2016)
14. Drew the block diagram of PPI (8279). DEC 2018
15. Draw the block diagram and explain the operations of 8251 serial communication interface. (DEC 2108)(June 2018)

UNIT – IV 8 BIT MICROCONTROLLER ARCHITECTERES AND PROGRAMMING

1. What is Microcontroller and Microcomputer?(Remembering)(CO4)

Microcontroller is a device that includes microprocessor, memory and I/O signal lines on a single chip, fabricated using VLSI technology. Microcomputer is a computer that is designed using microprocessor as its CPU. It includes microprocessor, memory and I/O.

2. What is mean by microcontroller? (Remembering) (CO4)

A device which contains the microprocessor with integrated peripherals like memory, serial ports, parallel ports, timer/counter, interrupt controller, data acquisition interfaces like ADC,DAC is called microcontroller.

3. List the features of 8051 microcontroller. (Remembering) (CO4) ***(Nov / Dec 2010)***

*single supply +5 volt operation using HMOS technology
* 4096 bytes program memory on chip (not on 8031)
*128 data memory on chip.
*Four register banks.
*Two multiple mode, 16-bit timer/counter.
*Extensive Boolean processing capabilities.
* 64 KB external RAM size
*32 bidirectional individually addressable I/O lines.
*8 bit CPU optimized for control applications.

4. Mention the purpose of 8251 chip. (Understanding) (CO4)

Intel's 8251A is a universal synchronous asynchronous receiver and transmitter compatible with Intel's Processors. This may be programmed to operate in any of the serial communication modes built into it. This chip converts the parallel data into a serial stream of bits suitable for serial transmission. It is also able to receive a serial stream of bits and converts it into parallel data bytes to be read by a microprocessor.

5. Name the special functions registers available in 8051. (Rem) (CO4) (June 2012,Dec 2014)

Accumulator, B Register, Program Status Word, Stack Pointer, Data Pointer, Port 0, Port1, Port 2, Port 3, Interrupt priority control register, Interrupt enable control register.

6. How many register banks are available in 8051 & how are they selected? (Understanding) (CO4) (May/June 2012, June 2014, Jan 2017*)*

There are 4 register banks namely bank0, bank1, bank 2 and bank3.

RS1	RS0	Bank Selection
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

7. Explain the function of the pins PSEN and EA of 8051. (Understanding) (CO4) (or)
Name of the pins that are used for external program memory accessing in 8051. (Nov / Dec 2011, May / June 2013, June 2014) (or)
Name the pin in 8051 that is tied high for execution of programs in internal memory. (Jun 2015) **PSEN**: PSEN stands for Program Store Enable. In 8051 based system in which an external ROM holds the program code, this pin is connected to the OE pin of the ROM. **EA**: EA stands for External Access. When the EA pin is connected to Vcc, program fetched to addresses 0000H through 0FFFH are directed to the internal ROM and program fetches to addresses 1000H through FFFFH are directed to external ROM/EPROM. When the EA pin is grounded, all addresses fetched by program are directed to the external ROM/EPROM.

8. Explain the 16-bit registers DPTR and SP of 8051. (US) (CO4) (Apr 2011, Jun 2015)

DPTR: DPTR stands for Data Pointer. DPTR consists of a high byte (DPH) and a low byte (DPL). Its function is to hold a 16-bit address. It may be manipulated as a 16-bit data register or as two independent 8-bit registers. It serves as a base register in indirect jumps, lookup table instructions and external data transfers**.**

SP: SP stands for Stack Pointer. SP is an 8- bit wide register. It is incremented before data is stored during PUSH and CALL instructions. The stack array can reside anywhere in on-chip RAM. The stack pointer is initialized to 07H after a reset. This causes the stack to begin at location 08H.

9. Illustrate the need of Port. (Understanding) (CO4)

The I/O devices are generally slow devices and their timing characteristics do not match with processor timings. Hence the I/O devices are connected to system bus through the ports.

10. What is the RAM & ROM size of 8051? (Remembering) (CO4)

Internal ROM or EPROM of **0 to 4K**. Internal RAM of **128 bytes**.

11. What is a port? (Remembering) (CO4)

The port is a buffered I/O, which is used to hold the data transmitted from the microprocessor to I/O device or vice-versa.

12. Explain the working of a handshake output port. (Understanding) (CO4)

In handshake output operation, the processor will load a data to port. When the port receives the data, it will inform the output device to collect the data. Once the output device accepts the data, the port will inform the processor that it is empty. Now the processor can load another data to port and the above process is repeated.

13. Explain the operating mode0 of 8051 serial ports. (Understanding) (CO4)

In this mode serial enters &exits through RXD, TXD outputs the shift clock.8 bits are transmitted/received:8 data bits(LSB first).The baud rate is fixed at 1/12 the oscillator frequency.

14. Explain the operating mode2 of 8051 serial ports. (Understanding) (CO4)

In this mode 11 bits are transmitted(through TXD)or received (through RXD):a start bit(0), 8 data bits(LSB first),a programmable 9th data bit ,& a stop bit(1).ON transmit the 9th data bit (TB* in SCON)can be assigned the value of 0 or 1.Or for eg:, the parity bit(P, in the PSW)could be moved into TB8.On receive the 9th data bit go in to the RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32or1/64 the oscillator frequency.

15. What is TXD? (Remembering) (CO4)

TXD: Transmitter Data Output. This output pin carries serial stream of the transmitted data bits along with other information like start bit, stop bits and priority bit.

16. What is RXD? (Remembering) (CO4)

RXD: Receive Data Input. This input pin of 8251A receives a composite stream of the data to be received by 8251A.

17. Explain the mode3 of 8051 serial ports. (Understanding) (CO4)

In this mode,11 bits are transmitted(through TXD)or received(through RXD):a start bit(0), 8 data bits(LSB first),a programmable 9th data bit ,& a stop bit(1).In fact ,Mode3 is the same as Mode2 in all respects except the baud rate. The baud rate in Mode3 is variable. In all the four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode0 by the condition RI=0&REN=1.Reception is initiated in other modes by the incoming start bit if REN=1.

18. What are the interrupts of 8051 microcontroller? **(Remembering) (CO4)** *(Nov / Dec 2010, May /June 2013)*

External interrupt 0 : IE0: 0003H
Timer interrupts 0 :TF0: 000BH
External interrupt 1 : IE1: 0013H
Timer Interrupt 1 : TF1: 001BH
Serial Interrupts:
1. Receive interrupt: RI: 0023H
2. Transmit interrupt: TI: 0023H

19. What are the different methods used for data transmission? (Remembering) (CO4)

The data transmission between two points involves unidirectional or bi-directional transmission of meaningful digital data through a medium. There are basically there modes of data transmission (a) Simplex (b) Duplex (c) Half Duplex.

In **simplex** mode, data is transmitted only in one direction over a single communication channel. For example; a computer (CPU) may transmit data for a CRT display unit in this mode.

In **duplex** mode, data may be transferred between two transceivers in both directions simultaneously.

In **half duplex** mode, on the other hand, data transmission may take place in either direction, but at a time data may be transmitted only in one direction. For example, a computer may communicate with a terminal in this mode. When the terminal sends data (i.e. terminal is sender). The message is received by the computer (i.e. the computer is receiver). However, it is not possible to transmit data from the computer to terminal and from terminal to the computer simultaneously.

20. What is the use of PCON register? (Remembering) (CO4)

The power mode control (PCON) special function register in the serial data input / output transmission, controls the data rates.

21. What is the use of SCON register? (Remembering) (CO4)

The serial port control (SCON) special function register in the serial data input / output transmission is used to controls data communication.

22. Compare Microprocessor and Microcontroller.(Analyzing)(CO4) (Dec 2009, Jun 2015, June 2016, Jan 2017 DEC 2018)

Sl.No	Microprocessor	Microcontroller
1	Microprocessor contains ALU, general purpose registers, stack pointer, program counter, clock timing circuit and interrupt circuit.	Microcontroller contains the circuitry of microprocessor and in addition it has built-in ROM, RAM, I/O devices, timers and counters.
2	It has many instructions to move data between memory and CPU.	It has one or two instructions to move Data between memory and CPU.
3	It has one or two bit handling instructions.	It has many bit handling instructions.
4	Access times for memory and I/O devices are more.	Less access time for built-in memory and I/O devices.
5	Microprocessor based system requires more hardware.	MC system requires less hardware reducing PCB size and increasing the reliability.
6	Concerned with rapid movement code and data from external addresses to the chip.	It is concerned with rapid movements of bits within the chip.
7	It must have many additional parts to be operational.	It can function as a computer with the addition of no external digital parts.

23. Give the alternate functions for the port pins of port3. (Remembering) (CO4) (Nov / Dec 2010, Jan 2016 DEC 2018)

RD – Read data control output. WR – Write data control output.
T1 – Timer / Counter1 external input or test pin.
T0 – Timer / Counter0 external input or test pin.
INT1 - Interrupt 1 input pin. INT 0 – Interrupt 0 input pin.
TXD – Transmit data pin for serial port in UART mode.
RXD - Receive data pin for serial port in UART mode.

24. Explain the register IE format of 8051. (Understanding) (CO4)

EA - Enable all control bit. ET2 - Timer 2 interrupt enable bit.
ES – Enable serial port control bit. ET1 – Enable Timer1 control bit.
EX1 - Enable external interrupt1 control bit. ET0 – Enable Timer0 control bit.
EX0 - Enable external interrupt0 control bit.

25. Give the format of PSW register of 8051. (Remembering) (CO4)(Jan 2016)

CY	AC	F0	RS1	RS0	OV	-	P

CY - Carry flag
AC - Auxiliary carry flag
F0 - User flag 0
RS1 - Register bank select bit1
RS0 - Register bank select bit 0
OV - Overflow flag
P - Parity flag. 1 – Odd parity

26. What is the use of TCON register? (Remembering) (CO4)

All the counter action is controlled by bit states in the timer / counter control register (TCON) and certain program instructions.

27. What is the bit pattern of IP in 8051 microcontroller?

-	-	PT2	PS	PT1	PX1	PT0	PX0

PT2 – Reserved for future use.
PS – Priority of serial port interrupts. Set / cleared by program.
PT1 – Priority of timer 1 overflow interrupt. Set / cleared by program.
PX1 – Priority of external interrupt 1. Set / cleared by program.
PT0 – Priority of timer 0 overflow interrupt. Set / cleared by program.
PX0 – Priority of external interrupt 0. Set / cleared by program.

28. What is the significant of GATE bit in TMOD control register? (Understanding) (CO4) (DEC 2018)

OR gate enable bit which controls RUN / STOP of timer 1/0. Set to 1 by program to enable timer to run if bit TR1/0 in TCON is set and signal on external interrupt INT 1/0 pin is high. Cleared to 0 by program to enable timer to run if bit TR1/0 in TCON is set.

29. What is the bit pattern of IE in 8051 microcontroller? (Remembering) (CO4)

EA	-	ET2	ES	ET1	EX1	ET0	EX0

EA – Enable interrupt bits. ET2 – Reserved for future use.
ES – Enable serial port interrupt. ET1 –Enable timer 1 overflow interrupt.
EX1 – Enable external interrupt 1 ET0 – Enable timer 0 overflow interrupt.
EX0 – Enable external interrupt 0.

30. What is the Interrupt Priority given in 8051 microcontroller? (Rem) (CO4) (Dec 2009)(DEC 2018)

IE0 – 0003H
TF0 – 000BH
IE1 – 0013H
TF1 – 001BH
SERIAL = RI OR TI – 0023H

31. What is the SFR address of TMOD, TCON, TL0, TH1, P0, SBUF? (Rem) (CO4)

TMOD – 89H
TCON – 88H
TL0 – 8AH
TH1 –8DH
P0 –80H
SBUF – 99H

32. Explain the MUL AB and DIV AB of 8051 microcontroller instructions. (Understanding) (CO4)

MUL AB – multiply the A and B register contents and place the 16-bit result in B and A. i.e., the lower byte is in A and upper byte is in B.

DIV AB – divide A and B. In dividing a byte by byte, the numerator must be in register A and the denominator must be in B. After the DIV instruction is performed, the quotient is in A and the remainder is in B.

33. List the addressing modes of 8051. (Remembering) (CO4) ***(Nov / Dec 2010)***

Direct addressing, Register addressing, and Register indirect addressing. Implicit addressing, Immediate addressing, Index addressing, Bit addressing.

34. Specify the single instruction, which clears the most significant bit of B register of 8051, without affecting the remaining bits. (Understanding) (CO4) (JUNE 2014)

Single instruction, which clears the most significant bit of B register of 8051, without affecting the remaining bits, is CLR B.7.

35. Develop an ALP to perform multiplication of 2 numbers using 8051.(Creating)(CO4)

```
MOV A,#data 1
MOV B,#data 2
MUL AB
MOV DPTR,#5000
MOV @DPTR,A(lower value)
INC DPTR
MOV A,B
MOVX @ DPTR,A
```

36. Develop a program to mask the 0th &7th bit using 8051. (Creating) (CO4)*(Nov / Dec 2010)*

```
MOV A,#data
ANL A,#81
MOV DPTR,#4500
MOVX @DPTR,A
LOOP SJMP LOOP
```

37. Write about CALL statement in 8051. (Remembering) (CO4)

There are two subroutine CALL instructions. They are *LCALL (Long CALL) and *ACALL (Absolute CALL) . Each increments the PC to the 1st byte of the instruction & pushes them in to the stack.

38. Write about the jump statement? (Remembering) (CO4) ***(Nov / Dec 2010)***

There are three forms of jump. They are **LJMP** (Long jump)-address 16, **AJMP** (Absolute Jump)-address 11 and **SJMP** (Short Jump)-relative address.

39. Develop an ALP to load accumulator, DPH, & DPL using 8051. (Creating) (CO4)

```
MOV A,#30
MOV DPH,A
MOV DPL,A
```

40. Develop an ALP to add 2 8-bit numbers using 8051. (Creating) (CO4)

```
MOV A,#30H
ADD A,#50H
```

41. What is the role of SWAP instruction available in 8051? (Remembering) (CO4) (June 2012)

MOV A, #12H: The immediate data 12 available in Accumulator.
SWAP A : 21 is available in Accumulator.

42. Develop an ALP to subtract 2 8-bit numbers &exchange the digits using 8051.(Creating) (CO4)

```
MOV A,#9F
MOV R0,#40
SUBB A,R0
SWAP A
```

43. Write a program to subtract the contents of R1 of Bank 0from the contents of R0 of Bank 2 using 8051. (Creating) (CO4)

```
MOV PSW,#10
MOV A,R0
MOV PSW,#00
SUBB A,R1
```

44. Explain DJNZ instructions of Intel 8051 microcontroller?(US)(CO4)(June 2014)

a) DJNZ Rn, rel - Decrement the content of the register Rn and jump if not zero.
b) DJNZ direct , rel - Decrement the content of direct 8-bit address and jump if not zero.

45.Write a program using 8051 assembly language to change the date 55H stored in the lower byte of the data pointer register to AAH using rotate instruction. (Creating) (CO4) (June 2014)

```
MOV DPL, #55H
MOV A, DPL
RL A
Label: SJMP label
```

46.List the instructions to load accumulator A, DPH and DPL with 30H. (Remembering) (CO4)

1) MOV A,#30 2)MOV DPH,A 3)MOV DPL,A

47. Explain the contents of the accumulator after the execution of the following program Segments. (Understanding) (CO4)

```
MOV A,#3CH
MOV R4,#66H
ANL A,R4
A 3C
R4 66
Ans : A = 24
```

48. Mention the advantage of register indirect addressing mode. (Understanding) (CO4)

It makes accessing data dynamic rather than static as in case of direct addressing mode.

49. What is the limitation of register indirect addressing mode in 8051 microcontroller?

R0 and R1 are the only registers that can be used for pointers in register indirect addressing mode. Since R0 and R1 are 8-bit wide, their use is limited to accessing any information in the internal RAM (scratch pad memory).

50. Write a program to clear 16 RAM locations starting at RAM address 60H. (Creating)(CO4)

```
        CLR     A
        MOV     R1, #60H
        MOV     R7, #16
AGAIN:  MOV     @R1, A
        INC     R1
        DJNZ    R7, AGAIN
```

51. Write a program to copy a block of 10 bytes of data from RAM locations starting at 35H to RAM locations starting at 60H. (Creating) (CO4)

```
        MOV     R0, #35H
        MOV     R1, #60H
        MOV     R3, #10
BACK:   MOV     A, @R0
        MOV     @R1, A
        INC     R0
        INC     R1
        DJNZ    R3, BACK
```

52. Explain the instruction MOV A, @R0. (Understanding) (CO4)

Move the contents of RAM location whose address is held by R0 into A.

53. Write a program to get the value of x from P1 and send x^2 to P2 continuously. (Creating) (CO4)

```
        MOV     DPTR, #300H     ORG   300H
        MOV     A, #0FFH              DB    0,1,4,9,16,25,36,49,64,81
        MOV     P1, A                 END
BACK:   MOV     A, P1
        MOVC    A, @A+DPTR
        MOV     P2, A
        SJMP    BACK
```

54. What address is assigned to register R2 of bank 0 and 2? (Remembering) (CO4)

The address assigned to register R2 of bank 0 and 2 are 02H and 12H respectively.

55. Write a program to find the 2's complement using 8051. (Creating) (CO4) ***(Nov / Dec 2010)***

```
MOV A,R0  ;(A)  <- R0
CPL A             ; 1s complement A
ADD A,#01  ; Add 1 to it to get 2s complement
```

56. Name some of the input output devices which are controlled by a microcontroller. (Remembering) (CO4) (Dec2010)

Keyboard, LCD, Stepper motor

57. What happens when a subroutine is called? (Analyzing) (CO4) (Nov/ Dec 2010)

When the subroutine is called, the control transferred to that subroutine, and the processor saves the content of program counter (PC) into stack and begins the fetch instructions from new location. After finishing execution of subroutine, the instruction RET transfers the control back to the caller. Every subroutine needs RET as last instruction.

58. What is the control word format of TMOD register? (Remembering) (CO4) (April / May 2011)(June 2018)

GATE	**C**/T	**M1**	**M0**	**GATE**	**C**/T	**M1**	**M0**
TIMER 1				**TIMER 0**			

GATE-**Gating control when set. The timer/counter**

C/T-Timer or counter selected cleared for timer operation

M0-Mode bit 0

M1-Mode bit 1

59. What are the operating modes in the timer of 8051? (Remembering) (CO4) (April 2011)

Four operating modes are available in timer they are

M1	M0	Mode	Operating Mode
0	0	0	13-bit timer mode
0	1	1	16-bit timer mode

1	0	2	8-bit Auto reload
1	1	3	Split timer mode

60. Define Polling. (Remembering) (CO4) (April / May 2011)

In polling the microcontroller continuously monitors the status of given device; when the status condition met, it performs the service after that, it moves on to monitor the next device until each one is serviced. Although polling can monitor the status of several devices and serve each of them as certain condition are met.

61. Difference between timer and counter of 8051. (Analyzing)(CO4)(Nov / Dec 2011)

8051 has two Timers/Counters. They can be used either as timers or counters.

Timers used to generate a time delay.

Counters to count events happening outside the microcontroller

62. How many register banks available in 8051 and how they are selected? (Understanding) (CO4) (May/Jun 2012)

There are four register bank in the 8051.They are selected in following method;

RS1	RS2	Register Bank
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

63. How do you calculate baud rate for serial communication for 8051? (Remembering) (CO4)

8051 receives and transfers data serially at many different baud rates.

Crystal oscillator frequency (11.059MHz) → divided by 12(Machine crystal freq) → divided by 32(UART)

64. What is the function of SM2 bit present in the SCON register in 8051? (Remembering) (CO4)

SM2 is a D5 bit of an SCON register. This enables the multiprocessing capability of the 8051,if SM=0 then the 8051 is not used in multiprocessor environment.

65. What is a serial data buffer? (Remembering) (Remembering) (CO4)

i).Serial data buffer is a special function register and it initiates serial transmission when byte is written to it and if read, it reads received serial data.

ii) It contains two independent registers internally.

iii) One of them is a transmit buffer, which is a parallel-in serial-out register. The other is a receive buffer, which is a serial-in parallel-out register.

PART-B (16 MARK QUESTIONS)

1. With neat sketch explain the architecture of 8051 microcontroller. (Understanding) (CO4) (Nov/Dec2010&Apr/May2011, May / June 2013,Jun 2015, Jan 2017 DEC 2018)
2. Explain the interrupt structure, SFR and timers of 8051. (Understanding) (CO4) Jan 2017
3. Explain I/O ports of 8051. (Understanding)(CO4)(June 2016)
4. Explain the timer / counter programming in 8051. (Understanding) (CO4) (May/June 2012, Jan 2016)
5. Briefly explain the interrupt available in 8051. (Understanding) (CO4) (May/June 2012, 2013, Jan 2017)
6. Explain the different serial communication modes in 8051. (Understanding) (CO4)(DEC 2018)
7. States various modes available for timer in 8051 and explain in details. (Remembering) (CO4) *(Apr/May2011)*
8. Explain the functional pin diagram of 8051 Microcontroller. (Understanding) (CO4) (June 2014)
9. Explain the addressing modes of 8051 MC with suitable example. (Understanding) (CO4) *(Nov / Dec 2010)& (May/June 2012, 2013, 2014*)
10. Explain how the memory is organized in 8051 family of controller. (Understanding) (CO4) (Jun 2015, 2016)
11. (a) How does the timer operate in 8051 in mode 2? Explain with suitable diagram. (b)Assuming XTAL = 11.0592 MHz, write an 8051 assembly language program to generate a square wave of 50 Hz frequency on pin P 2.3**.** (Creating) (CO4) (Jun 2015)
12. Explain how serial data communication is achieved in 8051 microcontroller. (Understanding) (CO4)

13. Explain in details the PSW and TMOD register formats. (Understanding) (CO4) (Dec 2014)
14. Draw the block diagram of 8051 microcontroller & write its unique features. (Remembering) (CO4)
15. Explain TCON, SCON, PCON & TMOD SFRs of 8051. (Understanding) (CO4)
16. Explain interrupt systems of 8051 microcontroller. (Understanding) (CO4) *(Nov / Dec 2010* Jan 2017*)*
17. With the help of example, explain the operation of timer interrupt programming and external hardware interrupt programming. (Understanding)(CO4)(Jan 2016)
18. a) Explain Memory organization of 8051. b) Explain Timer/Counter of 8051 in detail. (Understanding) (CO4)
19. Write a delay routine for 1 millisecond using timer 0 of 8051 for 12 MHz crystal frequency. (Creating) (CO4)
20. a) Calculate the reload value of timer 1 for achieving a baud rate of 4800 in 8051 for a crystal Frequency of 11.0592 M Hz. (Creating) (CO4)
    b) Write short description on register bank registers and their uses.
21. Explain the following instruction set of 8051 with examples. (Understanding) (CO4) (*Apr/May2011)*
22. Explain the following instructions of 8051 with examples. (Understanding) (CO4)
    i) CJNE destination, source, label ii) MUL AB, iii) RRL A, iv) SWAP A, v) SETB P2.0
23. Explain the following instructions of 8051. (Understanding) (CO4)
    i) MOV @R1,#05H, ii) XRL 15H, # 88H, iii) MOVX A, @DPTR, iv) SUBB A, # 20H,
    v) XCH A, R7
24. Develop an ALP to find a number that when XOR ed to the A register, results in the number 3FH in A. (Creating) (CO4)
25. Write a program to copy the bytes stored at 0100H to 0102H to internal RAM locations 20H to 22H. (Creating) (CO4)
26. i) Write 8051 ALP to read data from port1 when negative edge triggered at INTO and supply the data to port 2 by masking the upper 4 bits. (Creating) (CO4)
    ii) Write 8051 ALP to transmit 'Hello World' to PC at 9600 baud for external crystal frequency of 11.0592MHz. (Creating) (CO4)
27. Write a short note on Stack operations in 8051 microcontroller.
28. i)Write an 8051 ALP to find the average of given 2 & N numbers. (Creating) (CO4) *(Nov / Dec 2010)&*(*May/June 2012)*
    ii) Write an 8051 ALP to generate 50 ms delay. *(Nov / Dec 2010)*
29. What is the time taken to execute MUL instruction in 8051? (Remembering) (CO4)
30. Identify the addressing mode used by each of the following instruction.(Understanding)(CO4)
    i) MOV A, R4
    ii) MOVC A, @A+DPTR
    iii) SWAP A
    iv) MOV A, #30H
31. Write an ALP to find square of a number in 8051.(DEC 2018)

UNIT – V APPLICATIONS OF MICROPROCESSORS & MICROCONTROLLERS

1. Write an 8051 assembly language simple program to control stepper motor. (Creating) (CO5)

```
START :  MOV DI, 1200H
         MOV CX, 0004H
LOOP 1:  MOV AL,[DI]
         OUT 0C0,AL
         MOV DX, 1010H
L1 :     DEC DX
         JNZ L1
         INC DI
         LOOP LOOP1
         JMP START
        1200 : 09,05,06,0A
```

2. What is the EOI? (Remembering) (CO5)

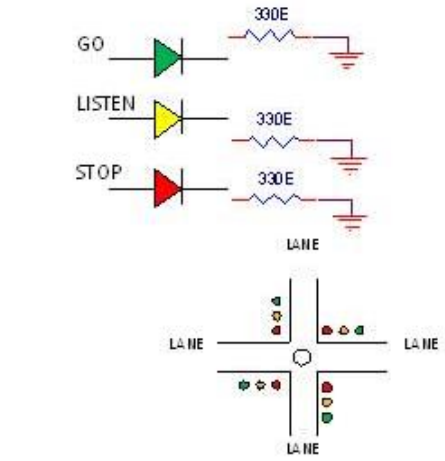
End of Interrupt(EOI)

The ISR bit can be reset by an End og Interrupt command issued by the MPU, usually just before exiting from the interrupt routine.

In the Fully Nested Mode, the highest level in the ISR would necessarily correspond to the last interrupt acknowledged and serviced. In such a case, a non-specific EOI command may be issued by the MPU.

However, if an FNM is not used, the 8259 may not be able to determine the last interrupt acknowledged. In such a case, a specific EOI command will have to be issued by the MPU.It should be noted that in the cascade mode, the EOI command must be issued twice, once for the master and once for the slave.

3. **Draw the diagram of traffic light control. (Remembering) (CO5)**



4. **What is meant by AEOI? (Remembering) (CO5)**

Automatic End of Interrupt (AEOI)

If the AEOI mode is set, the 8259 will perform a non-specific EOI on its own on the trailing edge of the third INTA pulse. The AEOI mode can only be used for a master 8259 and not for a slave.

5. **What is meant by stepper motor? (Remembering) (CO5)**

A stepper motor (or step motor) is a brushless DC electric motor that divides a full rotation into a number of equal steps. The motor's position can then be commanded to move and hold at one of these steps without any feedback sensor (an open-loop controller), as long as the motor is carefully sized to the application.

6. **What is meant by full step sequence? (Remembering) (CO5)**

In the full step sequence, two coils are energized at the same time and motor shaft rotates. The order in which coils has to be energized is given in the table below.

Full Mode Sequence

Step	A	B	A\	B\
0	1	1	0	0
1	0	1	1	0
2	0	0	1	1
3	1	0	0	1

7. **How many ports needed to in interfacing a stepper motor with microprocessor or microcontroller?(Analyzing) (CO5) (Jun 2015)**

Only one port is sufficient to operate the stepper motor in both processor as well as controller.

8. **How PWM used in the speed control of DC motor? (Understanding) (CO5)**

A pulse width modulator (PWM) is a device that may be used as an efficient light dimmer or DC motor speed controller. The circuit described here is for a general purpose device

that can control DC devices which draw up to a few amps of current. The circuit may be used in either 12 or 24 Volt systems with only a few minor wiring changes. This device has been used to control the brightness of an automotive tail lamp and as a motor speed control for small DC fans of the type used in computer power supplies.

9. What is the reason for replacing LCD over LED? (Understanding) (CO5)

- The declining prizes of LCD's,
- The ability to display numbers, characters and graphics
- Ease of programming for graphics

10. Define step angle. (Remembering) (CO5) (JUNE 2014)

The step angle is the minimum degrees of rotation with a single step. Various motor have different step angles

11. Differentiate unidirectional and bidirectional control of DC motor.(Analyzing) (CO5)

DC motor rotation for clockwise and counterclockwise (CCW) rotations. (Unidirectional)

12. What is ADC and DAC? (Remembering) (CO5) (JUNE 2014)

The electronic circuit that translates an analog signal into a digital signal is called analog-to-digital converter(ADC).

The electronic circuit translates a digital signal into an analog signal is called Digital-to-analog converter(DAC).

13. Define conversion time. (Remembering) (CO5)

It is defined as the total time required to convert an analog signal into a digital output. It is determined the conversion technique used and by the propagation delay in various circuits.

14. What are the functions to be performed by µp while interfacing an ADC? (Rem) (CO5)(DEC 2018)

i. Send a pulse to the START pin. ii. Wait until the end of conversion
iii. Read the digital signal at an input port.

15. Write the different types of ADC. (Remembering) (CO5)

i. Single slope ADC ii. Dual slope ADC iii. Successive approximation ADC
iv. Parallel comparator type ADC v. Counter type ADC

16. What is resolution time in ADC? (Remembering) (CO5)

It is defined as a ratio of change in value of input voltage Vi, needed to change the digital output by 1 LSB. If the full scale input voltage required tocause a digital output of all 1's is ViFS. Then the resolution can be given as

Resolution = $ViFS / (2^n-1)$

17. Differentiate parallel and serial ADC. (Remembering) (CO5)

Parallel ADC will have only 8 pins or more pins dedicated to bringing out the binary data.
Serial ADC will have only one pin for data out.

18. When is an external memory access generated in 8051? (Remembering) (CO5)

In 8051, during execution the data is fetched continuously. Most of the data is executed out of the 8051 built-in control store. When an address is outside the internal control store, an external memory access is generated.

19. Specify any two applications of Microcontrollers.(Remembering)(CO5)(June 2016)

(i) Traffic light control
(ii) Washing machine control

20 . **What are the hardware requirements to interface LCD to 8255.**

Flat ribbon cable, 8255 IC, LCD.

PART-B (16 MARK QUESTIONS)

1. Explain how to control the stepper motor using 8086.Also compile an ALP to changing the speed and direction of stepper motor using 8086 microprocessor. (Creating) (CO5) (May / June 2013,June 2014, Dec 2014, Jan 2016, June 2016, Jan 2017)
2. Draw a circuit diagram for the speed control of DC motor and write a program of direction control (Creating) (CO5) (June 2014)
3. Explain in the detail the process involved in the design of traffic light controller with example. (Understanding) (CO5) (Jun 2015, Jan 2017)
4. Explain how to interface LCD with 8051 microcontroller? (Understanding) (CO5) (May / June 2013, June 2014, Dec 2018)

5. Explain the interfacing of A to D and D to A converters. (Understanding) (CO5)(Jan 2016)(DEC 2018)
6. Explain in detail about the keyboard interfacing with the 8051 microcontroller. (Understanding) (CO5) (June 2014, DEC 2018)
7. With neat diagram explain interfacing of 8255 with 8051. (Remembering) (CO5)
8. Explain the technique involved in interfacing the external memory with the microcontroller. (Understanding) Jan 2017 (CO5)
9. Interface an 8*8 keyboard using 8255 ports and write a program to read the code of a pressed key. (Applying) (CO5)(June 2016)
10. Explain the interfacing of LCD with 8051 with diagram. (Dec 2018)
11.

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16EC414 Microprocessors and Microcontrollers - Cycle Test – I

Class: II ECE **Marks:25**

Part – A (Answer All Questions) **(5 x2= 10)**

1. Define microprocessor. (Remembering) (co1)
2. Recall the functions of bus and why address bus is unidirectional? (Remembering) (co1)
3. Summarize different flags available in 8085 microprocessor with its functions. (Understanding) (co1)
4. Compare and contrast the functions of control and status signals of 8085. (Analyzing) (co1)
5. Outline the functions of HOLD and HLDA in 8085 processor. (Understanding) (co1)

Part – B (Answer All Questions) **(15)**

6. Explain the architecture of 8085 with necessary diagram. (Understanding) (co1**) (8)**
7. What is addressing mode? Explain its type with an example. (Remembering) (co1) **(7)**

Cycle Test – II 16EC414 Microprocessors and Microcontrollers

Class: II ECE **Marks:25**

Part – A (Answer All Questions) **(5 x2= 10)**

1. Summarize the purpose of instruction queue. (Understanding,CO2)
2. List the merits of memory segmentation. (Remembering,CO2)
3. Inspect the processor which uses pipelined architecture and define pipelining. (Analyzing, CO2)
4. Name different flags available in 8086 microprocessor with its functions. (Remembering, CO2)
5. Construct the effective address using logical address of 8086 microprocessor. (Applying,CO2)

Part – B (Answer All Questions) **(7.5 x 2 = 15)**

6. Explain different types of addressing modes of 8086 with one example.(Understanding,CO2) **(8)**
7. Explain the functions of each block in the architecture 8086 microprocessor. (Understanding,CO2) **(7)**

16EC414 Microprocessors and Microcontrollers

Class : II ECE **Cycle Test – III**

Part – A (Answer All Questions) **(5 x 2 = 10)**

1. Identify the need for interfacing. (AP, CO3)(June 2015)
2. Recall the control word format of 8255? (R, CO3)
3. What is the difference between 2 key lockout and N key roll over modes in 8279? (U, CO3) (Nov/Dec 2011)
4. What is resolution and conversion time in ADC? (Remembering) (CO3)
5. Give the various modes of 8253 timer. (Remembering) (CO3)

Part – B (Answer All Questions) **(15)**

6. Draw and explain the internal blocks of 8255 with its modes. (Remembering, co3) **(7)**
7. List the major components of the 8279 keyboard/display interface and explain their functions with neat diagram. (U, CO3) (Nov-Dec 2009**).(8)**

16EC414 Microprocessors and Microcontrollers

Class : II ECE **Assignment – I**

Part – A (Answer All Questions) **(5 x 2 = 10)**

1. Compare Microprocessor and Microcontroller.(An, CO4) (Dec 2009, Jun 2015, June 2016)
2. How many register banks are available in 8051 & how are they selected? (U, CO4) (May/June 2012, June 2014)
3. Explain the function of the pins PSEN and EA of 8051. (U, CO4)
4. Give the alternate functions for the port pins of port3. (R, CO4) (Nov / Dec 2010, Jan 2016)
5. Explain the 16-bit registers DPTR and SP of 8051. (U, CO4) (Apr 2011, Jun 2015)

Part – B (Answer All Questions) **(15)**

6. With neat sketch explain the architecture of 8051 microcontroller. (U, CO4) (Nov/Dec2010&Apr/May2011, May / June 2013,Jun 2015**) (8)**
7. Explain the timer / counter programming in 8051. (U, CO4) (May/June 2012, Jan 2016) **(7)**

16EC414 Microprocessors and Microcontrollers

Class : II ECE **Assignment – II**

Part – A (Answer All Questions) **(5 x 2 = 10)**

1. How many ports needed to in interfacing a stepper motor with microprocessor or microcontroller?(An, CO5) (Jun 2015)
2. Define step angle. (R, CO5) (JUNE 2014)
3. What are the functions to be performed by µp while interfacing an ADC? (R, CO5)
4. Specify any two applications of Microcontrollers.(R, CO5)(June 2016)
5. What is the reason for replacing LCD over LED? (U, CO5)

Part – B (Answer All Questions) **(15)**

6. Explain how to control the stepper motor using 8086.Also compile an ALP to changing the speed and direction of stepper motor using 8086 microprocessor. (C, CO5) (May / June 2013,June 2014, Dec 2014, Jan 2016, June 2016)**(8)**
7. Explain in the detail the process involved in the design of traffic light controller with example. (U, CO5) (Jun 2015**)(7)**