K.S.R. COLLEGE OF ENGINEERING(Autonomous)

Vision of the Institution

- We envision to achieve status as an excellent educational institution in the global knowledge hub, making self-learners, experts, ethical and responsible engineers, technologists, scientists, managers, administrators and entrepreneurs who will significantly contribute to research and environment friendly sustainable growth of the nation and the world.

Mission of the Institution

- To inculcate in the students self-learning abilities that enable them to become competitive and considerate engineers, technologists, scientists, managers, administrators and entrepreneurs by diligently imparting the best of education, nurturing environmental and social needs.
- To foster and maintain a mutually beneficial partnership with global industries and Institutions through knowledge sharing, collaborative research and innovation.

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Vision of the Department

- To create ever green professionals for software industry, academicians for knowledge cultivation and researchers for contemporary society modernization.

Mission of the Department

- To produce proficient design, code and system engineers for software development.
- To keep updated contemporary technology and fore coming challenges for welfare of the society.

Programme Educational Objectives (PEOs)

PEO1 : Figure out, formulate, analyze typical problems and develop effective solutions by imparting the idea and principles of science, mathematics, engineering fundamentals and computing.

PEO2 : Competent professionally and successful in their chosen career through life-long learning.

PEO3 : Excel individually or as member of a team in carrying out projects and exhibit social needs and follow professional ethics.

K.S.R. COLLEGE OF ENGINEERING(Autonomous)

Department of Computer Science and Engineering

Subject Name: Computer Organization and Architecture
Subject Code: 18CS312 **Year/Semester: II/III**

Course Outcomes: On completion of this course, the student will be able to

CO1 Demonstrate the instruction sets with various addressing modes.
CO2 Know how to generate control signals using control units.
CO3 Understand pipelining concepts.
CO4 Determine the performance of memory in commercial processor.
CO5 Know how to organize I/O devices.

Program Outcomes (POs) and Program Specific Outcomes (PSOs)

A. Program Outcomes (POs)

Engineering Graduates will be able to :

PO1 **Engineering knowledge:** Ability to exhibit the knowledge of mathematics, science, engineering fundamentals and programming skills to solve problems in computer science.

PO2 **Problem analysis:** Talent to identify, formulate, analyze and solve complex engineering problems with the knowledge of computer science. .

PO3 **Design/development of solutions:** Capability to design, implement, and evaluate a computer based system, process, component or program to meet desired needs.

PO4 **Conduct investigations of complex problems:** Potential to conduct investigation of complex problems by methods that include appropriate experiments, analysis and synthesis of information in order to reach valid conclusions.

PO5 **Modern tool Usage:** Ability to create, select, and apply appropriate techniques, resources and modern engineering tools to solve complex engineering problems.

PO6 **The engineer and society:** Skill to acquire the broad education necessary to understand the impact of engineering solutions on a global economic, environmental, social, political, ethical, health and safety.

PO7 **Environmental and sustainability:** Ability to understand the impact of the professional engineering solutions in societal and Environmental contexts and demonstrate the knowledge of, and need for sustainable development.

PO8 **Ethics:** Apply ethical principles and commit to professional ethics and responsibility and norms of the engineering practices.

PO9 **Individual and team work:** Ability to function individually as well as on multi-disciplinary teams.

PO10 **Communication:** Ability to communicate effectively in both verbal and written mode to excel in the career.

PO11 **Project management and finance:** Ability to integrate the knowledge of engineering and management principles to work as a member and leader in a team on diverse projects.

PO12 **Life-long learning:** Ability to recognize the need of technological change by independent and life-long learning.

B. Program Specific Outcomes (PSOs)

PSO1 Develop and Implement computer solutions that accomplish goals to the industry, government or research by exploring new technologies.

PSO2 Grow intellectually and professionally in the chosen field.

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

18CS312 – COMPUTER ORGANIZATION AND ARCHITECTURE

UNIT 1

BASIC STRUCTURE OF COMPUTERS

PART-A

2 MARKS

1. Define Computer Architecture. (Understanding)

Computer Architecture refers to the attributes of a system visible to a programmer or the attributes that have a direct impact on the logical execution of a program.

Examples of architectural attributes:

1. Instruction Set
2. The number of bits used to represent various data types (numbers, characters)
3. IO mechanisms & techniques for addressing memory.

2. Define Computer Organization. (Understanding)

Computer organization refers to the operational units and their inter connections that realize the architectural specifications.

Example for Organizational attributes:

Hardware details transparent to the programmer such as

- Control signals,
- Interface between the computer & Peripherals and the memory technology used.

3. What is the difference between Computer Architecture and Computer Organization ? (Understanding)

S.No	Computer Architecture	Computer Organization
1.	It refers to the attributes that have a direct impact on the logical execution of the program.	It refers to the operational units and their interconnections that realize the architectural specifications
2.	Architectural attributes includes the Instruction set, data types, no of bits used to represent the data, I/O mechanisms.	Organizational attributes include those h/w details such as control signals, interfaces b/w the computer memory & I/O peripherals

4. What is cache memory? (Understanding)

The small and fast RAM units are called as caches. When the execution of an instruction calls for data located in the main memory, the data are fetched and a copy is placed in the cache. Later if the same data is required it is read directly from the cache.

5. What is the function of ALU? (Understanding)

Most of the computer operations (arithmetic & logic) are performed in ALU. The data required for the operation is brought by the processor and the operation is performed by the ALU.

6. What is the function of control unit? (Understanding)

The Control unit is the main part of the computer that coordinates the entire computer operations. That is the speed of the input device is slower than the processor speed. So we must coordinate this speed differences. It issues timings signals that controls the data transfer.

7. What are basic operations of a computer memory? (Understanding)

The basic operations of the memory are READ and WRITE.

READ – read the data from input device to memory.

WRITE – writes data to the output device.

8. List out the operations of the computer.(Applying)

The computer accepts the information in the form of programs and data through an input unit and stores it in the memory.

1. Information stored in the memory is fetched under program control into an arithmetic and logic unit where it is processed.
2. Processed information leaves the computer through an output unit.
3. All activities inside the machine are directed by the control unit.

9. What are the main elements of a computer? (Understanding)

Processor: To interpret and execute programs

Memory: For storing programs and data

Input-output equipment: For transferring information between the computer and outside world.

10. Define Computer design. (Understanding)

It is concerned with the hardware design of the computer. Once the computer specifications are formulated, it is the task of the designer to develop hardware for the system. Computer design is concerned with the determination of what hardware should be used and how the parts should be connected. This aspect of computer hardware is sometimes referred to as computer implementation.

11. Define Stored Programmed Concept. (Understanding)

- Storing program and their data in the same high-speed memory.
- It enables a program to modify its own instructions (such self-modifying Programs have undesirable aspects, however and are rarely used.)

12. What are the registers generally contained in the processor?(Remembering)

MAR – Memory Address Register.

MDR – Memory Data Register.

IR – Instruction Register.

R_0 – Rn – General purpose Register.

PC – Program Counter.

13. What do you mean by Memory address register(MAR) and Memory data register(MDR)?

The MAR holds the address of the location to be accessed. The MDR contains the data to be written into or read out of the addressed location.

14. Define Interrupt and ISR. (Understanding)

An Interrupt is a request from an I/O device for service by the processor. The Processor provides the requested service by executing the interrupt service routine. Due to this diversion the internal state of the processor must be saved in memory location before servicing the interrupt.

15. Define Bus. (Understanding)

A Group of lines that serves as a connecting path for several devices is called a bus. In addition to the lines that carry the data, address and control lines.

16. Compare single bus structure and multiple bus structure. (Applying)

A system that contains only one bus (i.e. only one transfer at a time) is called as a single bus structure. Advantage: low cost & flexibility.

A system contains multiple buses called as multiple bus structure. This allows two or more transfers to be carried out at the same time. It will give better performance, but the cost is very high.

17. What is System software? Give an example. (Understanding)

It is a collection of programs that are executed as needed to perform functions such as

1. Receiving and interpreting user commands.
2. Entering and editing application programs and storing them as files in secondary storage devices.
   Eg. Assembler, Linker, Compiler etc.

18. What is Application software? Give an Example. (Understanding)

Application programs are usually written in high level programming language, in which them programmer specifies mathematical and text processing operations. These operations are described a format that is independent of the particular computer used to execute the program.

Eg. C, C++, java.

19. What are the two techniques used to increase the clock rate R? (Understanding)

The two techniques used to increase the clock rate R are:

1. The integrated – circuit (IC) technology can be increased which reduces the time needed to complete a basic step.
2. We can reduce the amount of processing done in the basic step.

20. What is Multiprogramming or multi tasking? (Understanding)

The OS manages the concurrent execution of several application programs to make the best possible uses of computer resources. This pattern of concurrent execution is called multiprogramming or multitasking.

21. What is elapsed time of computer system? (Understanding)

The total time to execute the total program is called elapsed time. It is affected by the speed of the processor, the disk and the printer.

22. What is processor time of a program? (Understanding)

The period during which the processor is active is called processor time of a program. It depends on the hardware involved in the execution of individual machine instructions.

23. Define clock rate. (Understanding)

The clock rate is given by,

R=1/P, where P is the length of one clock. It can be measure as cycles per second (Hertz).

24. What is meant by clock cycle? (Understanding)

Processor circuit is controlled by a timing signal called a clock. The clock defines regular time intervals, called clock cycle. To execute the machine instruction the processor divides the action to be performed into sequence of basic steps; each step can be completed in one clock cycle.

25. Write down the basic performance equation. (Remembering)

T=N*S/R

T-Processor time

N-Number of machine instructions

S-Number of basic steps needed to execute one machine instruction

R-Clock rate

26. What is addressing mode? (Understanding)

The addressing mode is defined as the different ways in which the location of an operand is specified in an instruction.

27. What are the different types of addressing modes available? (Understanding)

The different types of addressing modes are:

1. Immediate addressing mode
2. Register addressing mode
3. Direct or absolute addressing mode
4. Indirect addressing mode
5. Indexed addressing mode
6. Relative addressing mode
7. Auto increment
8. Auto decrement

28. Define Register addressing mode. (Understanding)

In register addressing mode, the operand is the contents of a processor register. The name (address) of the register is given in the instruction.

Effective address (EA) = Ri, Where Ri is a processor register.

29. Define absolute addressing mode. (Understanding)

In absolute addressing mode, the operand is in a memory location. The addresses of this location are given explicitly in the instruction. This is also called as direct addressing mode.

EA = Loc Where loc is the memory address.

30. What is relative addressing mode? (Understanding)

The Effective address is determined by the index mode using the program counter in place of general purpose register. This mode is used to access the data operands.

EA = X + [PC]

31. What is indirect addressing mode? (Understanding)

The Effective address of the operand is the contents of a register or memory location whose address appears in the instruction EA = [Ri] or EA = [Loc].

32. What is indexed addressing mode? (Understanding)

The Effective address of the operand is generated by adding a constant value to the contents of a register. EA = X + [Ri].

33. Define auto increment mode of addressing. (Understanding)

The Effective address of the operand is the contents of a register specified in the instruction. After accessing the operand, the contents of this register are automatically incremented to point to the next item in the list. EA = (Ri) +

34. Define auto decrement mode of addressing. (Understanding)

The contents of a register specified in the instruction are first automatically decremented and are then used as the effective address of the operand. EA = - (Ri)

35. List the basic instruction types.(Applying)

The various instruction types are,

1. Three address instructions
2. Two-address instructions
3. Single-address instructions
4. Zero-address instructions

36. Define Device interface. (Understanding)

The butter registers DATAIN and DATAOUT and the status flags SIN and SOUT are part of circuitry commonly known as a device interface.

37. What are the various ways of representing signed integers in the system? (Understanding)

1. Sign and magnitude system
2. 1’s complement system
3. 2’s complement system

38. Name 5 parts of the computer. (Remembering)

1. Input
2. Memory
3. Arithmetic and logic
4. Output and
5. Control units.

39. List the parts of CPU of IAS computer. (Understanding)

i) Program Control Unit (PCU): It is responsible for fetching instructions from main memory and interpreting them.

ii) Data Processing Unit (DPU): It is responsible for executing instructions.

40. What is register? (Understanding)

A small set of high-speed storage devices called registers, which serve as implicit storage locations for operands and results.

41. List the major components of PCU. (Remembering)

Instruction Register (IR): It stores the opcode of the instruction that is currently being executed.

Program Counter (PC): It automatically stores and keeps track of the address of the next instruction to be executed.

Address Register (AR): It holds the address of a data operand to be fetched from or sent to main memory.

Instruction Buffer Register (IBR): IAS has the feature of fetching two instructions at a time from memory. Instruction Buffer register holds the second instruction.

42. What is multiprocessor? (Understanding)

A technique which allows instructions from different program to be executed simultaneously, employs a computer with more than one CPU, such a computer is called a multiprocessor.

43. List the phases, which are included in the each instruction cycle. (Applying)

Fetch: fetches instruction from main memory (M)

Decode: decodes the instruction's opcode

Load: loads (read)from M any operands needed unless they are already in CPU Registers

Execute: Executes the instruction via a register-to-register operation using an appropriate functional unit of the CPU such as a fixed–point adder.

Store: Stores(write)the results in M unless they are to be retained in CPU register.

44. What are the types of computer? (Understanding)

1. Mini computer
2. Micro computers
3. Mainframe computers
4. Super computers

45. What are the two major steps in processing an instruction? (Understanding)

Fetch step: During this step a new instruction is read from the external memory M by the PCU.

Execute step: During this step operations specified by the instruction are executed by the DPU.

46. What is CPU clock time? (Understanding)

The actions of the CPU during an instruction cycle are defined by a sequence of micro operations, each of which involves a register-transfer operation. The time taken by the smallest CPU micro operation is the CPU cycle time or CPU's clock period T clock.

47. What are the speedup techniques available to increase the performance of a computer?

Cache: It is a fast accessible memory often placed on the same chip as the CPU. It is used to reduce the average time required to access an instruction or data to a single clock cycle.

Pipelining: Allows the processing of several instructions to be partially overlapped.

Super scalar: Allows processing of several instructions in parallel (full overlapping)

48. What are the major attributes of RISC? (Understanding)

- Relatively few instruction types and addressing modes.
- Fixed and easily decoded instruction formats.
- Fast and single cycle execution.
- Hard wired rather than micro programmed control
- Memory access limited mainly to load/store instruction.
- Use of compilers to optimize object-code performance.

49. Differentiate between RISC and CISC (Applying)

RISC	CISC
1.Simple Instruction can be processed in one clock cycle	1.Complex instruction require more cycles per instruction
2. Number of instructions is more	2. Less Number of Instructions
3. Instructions have fixed format	3. Variable format
4. Instruction occupy 32 bits	4. Instruction occupy 2 bytes to 10 bytes

50. What are Timing signals? (Understanding)

Timing signals are signals that determine when a given action is to take place. Data transfers between the processor and the memory are also controlled by the control unit through timing signals.

PART- B

1. Draw and explain the block diagram of a simple computer with five functional units **(Applying)**
2. Explain the various addressing modes. **(Understanding)**
3. Discuss in detail the various performance measures of a computer **(Understanding)**
4. Explain in detail the data transfer between the memory & I/O unit. **(Understanding)**
5. Explain the different types of Bus Structures. **(Understanding)**
6 Write short notes on RISC and CISC. **(Understanding)**
7. Mention the rules for floating point addition and subtraction and explain how they are implemented? **(Applying)**
8. Explain the various types of Addressing modes with example. **(Understanding)**
9. Write short notes on fixed point and floating-point numbers of data representation? Explain the instruction and its types with examples? **(Applying)**
10. Explain the basic operational concepts of a processor. **(Understanding)**
11. Briefly explain the classification of Instruction set Architectures. **(Understanding)**
12. Explain the basic instruction types and Instruction sequencing. **(Understanding)**

UNIT II

BASIC PROCESSING UNIT
PART-A
2 MARKS

1. What do you mean by micro-operation? (Understanding)

To perform fetch, decode and execute cycles the processor unit has to perform set of operations called **micro-operation.**

2. Define Processor. (Understanding)

It executes machine instructions and coordinates the activities of other units. It is also called as instruction set processor or central processing unit (CPU).

3. What is Data path? (Understanding)

The data registers, ALU and the interconnecting bus is referred to as **data path.**

4. What is meant by program counter? (Understanding)

It is a processor register mainly used for execution. It stores the address of the next instruction to be executed. After fetching an instruction the content of the PC are updated to point to the next instruction in the sequence.

5. Define IR. (Understanding)

IR is an instruction register. To execute an instruction the processor fetches the contents of the memory location pointed by the PC. The contents of this location are interpreted as an instruction to be executed. They are loaded into the IR.

6. What is micro program? (Understanding)

A sequence of one or more micro operations designed to control specific operation, such as addition ,multiplication is called a **micro program** .

7.What do you mean by hardwired control unit? (Understanding)

In the hardwired control ,the control units use fixed logic circuits to interpret instructions and generate control signals from them.

8.Define microinstruction. (Understanding)

It is to assign one bit position to each control signal required in the CPU. However, This scheme has one serious drawback –assigning individual bits to each control signal results in long micro instructions ,because the number of required signal is usually large. moreover ,only few bits are used in any given instruction .The solution of this problem is to group the control signals.

9. List the two techniques used for grouping of control signals.(Applying)

1.**Control signals**: IN and OUT signals

2.**Gatin signals** : Read, write ,clear A ,set carry in, continue operation etc.

10.Write down the steps to execute an instruction.(Remebering)

- Fetch the contents of the memory location pointed by the PC and store that content into instruction registers. IR← ╔ PC ╗
- Increment the PC value by 4 to point out the next instruction in the program. PC←[PC]+4
- Carry out the actions specified by the instruction in the IR.

11.Define fetch step. (Understanding)

To perform the execution of the instruction we have to fetch the content from the memory and store that content into the processor register IR.. This is known as fetching phase.

12.What is meant by execution phase? (Understanding)

Carry out the actions specified by the instruction in the instruction in the instruction register is known as execution instruction

13.Define MAR, MDR. (Understanding)

MAR means memory address register and MDR means memory data registers. These two are the processor registers that can be used in memory read and write operations.

14.Define register transfer and list out the signals used to do it. (Understanding)

As instruction execution involves a sequence of steps in which data are transferred from one register to another register. Two control signals are used to place the contents of the registers on the bus or to load the data on the bus into the registers. The signals are Ri in, Ri out.

15.Write down the control sequence for Move (R1), R2. (Understanding)

The control sequence is:

R1 out, MAR in Read

MDRoutE, WMFC

MDRout,R2 in,

16.Write down the steps to transfer the content of register R1 to register R4. (Understanding)

- Enable the output of register R1 by setting R1 out to 1. This places the contents of R1 on the processor bus.
- Enable the input of register R4 by setting R4 into 1. This loads data from processor bus into register R4.

17.Define multiphase clocking. (Understanding)

In some processor data transfers may use both the rising and falling edges of the clock. Two or more clock signals are needed to guarantee proper transfer of data. This is known as multiphase clocking.

18.Define MFC signal. (Understanding)

To accommodate the validity in response time, the processor waits until it receives an indication that the requested Read operation has been completed. A control signal MFC(Memory Function Complete) is used for this purpose.

19.Write down the steps to execute Add(R3),R1 instruction. (Understanding)

- Fetch the instruction
- Fetch the first operand
- Perform the addition
- Load the result into R1.

20.Define register file. (Understanding)

In multi bus architecture all the general purpose registers are called combined into a single clock called as register file.

21.Define interrupt. (Understanding)

CPU supervises the other system components via special control lines. Whenever the CPU receives the signals from the IO device (i.e.) interrupt signals, it suspends the current execution of the program and performs the interrupt request. After process the interrupt request, CPU transfers from supervisor mode to user mode.

22.Define instruction cycle. (Understanding)

The sequence of operations involved in processing an instruction is called as an instruction cycle. It is divided into two phases: 1.fetch cycle 2. execution cycle. The instruction is obtained from main memory during the fetch cycle. The execution cycle includes decoding the instruction, fetching any required operands, and performing the operation specified by the instructions opcode.

23.Define Hardwired control . (Understanding)

The circuit is design with the useful goals of minimizing the number of components used and maximizing the speed of operation. Once the unit is constructed, the only way implement changes in control unit behaviors *are* by redesigning the entire unit. Such a circuit is called hardwired control design.

24.What is the difference between hardwired control and micro' programmed control memory? (Understanding)

- **Hardwired Control**: Implementation of hardwired is using sequential circuits and flip flops. If any change is to be done then the whole design is to be modified.
- **Micro Program Control**: Micro program is based on microinstruction. If the change is *to* be design then part of program is *to* be modified.

25.What is the difference between horizontal microinstructions and vertical microinstructions? (Understanding)

- **Horizontal Micro Instruction**: Ability to express a high degree of parallelism. The length of format is long.Little encoding of control information.
- **Vertical Micro Instruction**: The length of the format is short Limited ability *to* express parallel micro operations. Considerable encoding of control information

26.Define multicycle. (Understanding)

ALU processes each m bit slice in K consecutive clock cycles is termed as multicycle.

27.Explain load-store architecture? (Understanding)

The program fragment that uses only the "load and store instruction to access memory is called load and store architecture. It is common to allow other instruction to specify operands in memory.

28.How do you measure the speed of a pipeline? (Understanding)

Pipeline speedup s(m) = T(1)1T(m) ,

m -Stage ...

T(m) - The execution time for same target workload on an m-stage pipeline

T(1) - The execute on time for same target workload on a non pipelined processor

29. How do you calculate the performance of the pipeline? (Understanding)

Pipeline's performance *I* cost ratio PCR = *f/k*

f - Clock frequency k - Hardware cost

30.Define Hit ratio. (Understanding)

The performance of cache memory is frequently measured in terms of a quantity called hit ratio. Let N1 and N2 denote the number of references to M1 and M2respectively in the block address stream.The block hit ratio H is defined by H=N1/N1+N2

31.What is the difference between macro and microinstructions? (Understanding)

Macro Instruction: Assign symbolic name to sequence of instructions I

Micro Instruction: Specify low-level micro operations.

32.Explain coprocessor function? (Understanding)

Coprocessor is a separate instruction set processor (ie) closely coupled to the CPU and whose instruction and registers direct extensions of the CPU'S.

33.What is control word? (Understanding)

It is a word whose individual bits represent the various control signals. Control sequence of an instruction defines a unique combination of 1's and 0' s in the control word.

A sequence of CW's corresponding to the control sequence of a machine Instruction constitute the micro routine for that instruction.

34.Define control store. (Understanding)

The micro routines for all instructions in the instructions set of a computer are stored in a special memory called the control store. To read the control words sequentially from the control store, a micro program counter is used.

35.List out the situations that not increment the micro Pc value. (Applying)

- When a new instruction is loaded into the IR , the micro PC is loaded with the starting address of the micro routine for that instruction.
- When a branch instruction is encountered and the branch condition is satisfied the micro Pc is loaded with the micro Pc is loaded with the branch target address.
- When an End instruction is encountered micro Pc is loaded with the address of the first CW in the micro routine for the instruction fetch cycle.

36.What is the draw back present in micro instruction s representation and how can we eliminate it? (Understanding)

Assigning individual bits to each control signal results in long micro instruction s because the number of required signals is usually large. Moreover only a few bits are set 1. So the available bit space is poorly used. We can overcome this draw back by grouping the relevant control signals.

37.Define vertical organization. (Understanding)

Highly encoded scheme groups more number of instruction s into a single group. So minimum number of groups is enough to represent instruction set. This is known as vertical organization.

38.What is meant by horizontal organization? (Understanding)

Minimally encoded scheme groups minimum number of instruction s into single group. So we need more group to represent the instruction set. This is known as vertical organization.

39.Define bit ORing technique. (Understanding)

By using this technique we can modify the branch address. It use an Or gate to change the least significant bit of the specified instruction's address to1 , if the addressing mode is used.

40.Why it is need of pre fetch instruction?(Remebering)

One draw back of micro programmed control is the slower operation because of the time it takes to fetch instruction s from the control store. Faster operation is achieved if the next instruction is pre fetched while three current one is being executed.

41.Define emulation. (Understanding)

Programs written in the machine language of M2 can be run on computer M1 that is M1 emulate M2. Emulation allows us to replace absolute equipments.

42.What is meant by micro programmed control? (Understanding)

In some processor the control signals are generated by a program similar to machine language programs. This is known as micro programmed control.

43.Comparison between Hardwired and Micro programmed control (Creating)

Attribute	**Hardwired control**	**Micro programmed control**
Speed	Fast	slow
Ability to handle large	Some what difficult	Easier
Design process	Some what complicated	Orderly and systematic
Applications	Mostly RISC microprocessors	Mainframe ,some microprocessors

PART- B

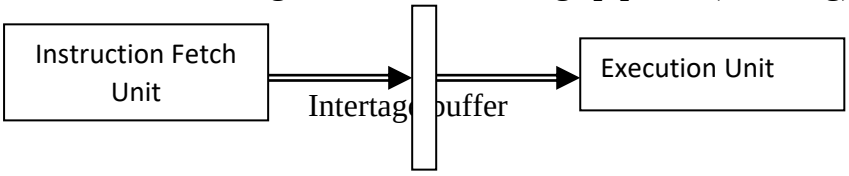
1.Give the basic organization of a Microprogrammed control unit. Draw a flowchart of a micro routine for the instruction Add Src, Rdst. **(Understanding)**
2.Draw the organization of a single-bus processor (**Creating)**
3.Give the control sequences for fetching a word from memory, storing a word in memory,. **(Understanding)**
3.Explain the basic organization of a Hardwired control unit. Mention its advantages and disadvantages**(Understanding)**.
4. Explain multiple bus organization**(Understanding)**
5. Explain nano programming**(Understanding)**
6.Explain the execution of a complete instruction with the help of an example. **(Understanding)**

UNIT III
PIPELINING
PART-A
2 Marks

1.Define pipelining(Understanding)

By arranging the hardware we can perform more than one instruction at the same time. The number of operations performed per second is increased with out changing the elapsed time. This is called pipelining.

2. Draw the hardware organization of two-stage pipeline.(Creating)



3.What are the steps in pipelining processor. (Understanding)

Fetch : Read the instruction from the memory.

Decode : Decode the instruction and fetch the source operands.

Execute : Perform the operation specified by the instruction

Write : Store the result in the destination location.

4. Write short notes on instruction pipelining.(Applying)

The various cycles involved in the instruction cycle. These fetch, decode and execute cycles for several instructions are performed simultaneously to reduce overall processing time. This process is referred as **instruction pipelining.**

5.What is the need to use the cache memory in pipelining concept? (Understanding)

Each stage in a pipeline is expected to complete its operation in one clock cycle. But the accessing time of the main memory is high. So it will take more than one clock cycle to complete its operation. So we are using cache memory for pipelining concept. The accessing speed of the cache memory is very high.

6. Define Structural hazards. (Understanding)

These hazards are because of conflicts due to insufficient resources when even with all possible combination, it may not be possible to overlap the operation.

7. What are the types of hazards? (Understanding)

1. Structural hazards
2. Data or Data dependent hazards
3. Instruction or control hazards

8.What is Data hazard? (Understanding)

A data hazard is any condition in which either the source or the destination operands of an instruction are not available at the time expected in pipeline. As a result some operation has be delayed and the pipeline stalls.

9. What are instruction hazards? (Understanding)

They arise while pipelining branch and other instructions that change the contents of program counter. The simplest way to handle these hazards is to stall the pipeline stalling of the pipeline allows few instructions to proceed to completion while stopping the execution of those which results in hazards

10. What is meant by bubbles in pipeline? (Understanding)

Any condition that causes the pipeline to be is known as pipeline stall. This is also known as bubble in the pipeline. Once the bubble is created as a result of a delay, a bubble moves down stream until it reaches the last unit.

11. What is structural hazard? (Understanding)

When two instructions require the use of a given hardware resource at the same time this hazard will occur. The most common case of this hazard is memory access.

12. How can we eliminate the delay in data hazard?(Remebering)

In pipelining the data can be executed after the completion of the fetch operation. The data are available at the output of the ALU once the execute stage completes. Hence the delay can be reduced if we arrange for the result of fetch instruction to be forwarded directly for use in next step. This is known as operand forwarding.

13. How can we eliminate data hazard using software? (Remebering)

The data dependencies can be handled with the software. The compiler can be used for this purpose. The compiler can introduce the two cycle delay needed between instruction I1 and I2 by inserting NOP (no operation)

```
I1:   MUL  R2, R3, R4
      NOP
      NOP
I2:   ADD  R5, R4, R6
```

14. When will the instruction have side effect? (Remebering)

Some time an instruction changes the contents of a register other than the destination. An instruction that uses an auto increment or auto decrement addressing mode is an example. AddWithCarry R2, R4

This instruction will take the carry value present in the condition code register. So it refers the register which is not represented in the instruction

15. Define branch penalty. (Remebering)

The time lost as a result of a branch instruction is often referred to as the branch penalty. This will cause the pipeline to stall. So we can reduce branch penalty by calculating the branch address in early stage.

16. What is the use of instruction queue in pipeline? (Remebering)

Many processors can fetch the instruction before they are needed and put them in queue called instruction queue. This instruction queue can store several instructions.

17. Define dispatch unit. (Remebering)

It is manly used in pipeline concept. It takes the instruction from the front of the instruction queue and sends them to the execute unit for execution.

18. What is meant by branch folding and what is condition to implement it? (Remebering)

The instruction fetch unit has executed the branch instruction concurrently with in the execution of other instruction s. This occurs only if at the time of branch is encountered at least one instruction is available in the queue than the branch instruction.

19. What is meant by delay branch slot? (Remebering)

A location following branch instruction is called as branch delay slot. There may be more than one branch delay slot, depending on the execution time. The instruction in the delay slot is always fetched and at least partially execution before the branch decision is made.

20. Define delayed branching. (Remebering)

It is a technique by using it we can handle the delay branch slot instructions. We can place some useful instruction in the branch delay slot and execute these instruction s when the processor is executing the branch instruction. If there is no useful instruction in the program we can simply place NOP instruction in delay slot. This technique will minimize the branch penalty.

21. Define prediction. (Remebering)

It is a technique used for reducing branch penalty associated with the condition branches. Assume that the branch will not take place and to continue the fetch instructions in sequential address order until the branch condition is evaluated.

22. Define static and dynamic branch prediction. (Remebering)

The branch prediction decision is always the same every time a given instruction is executed. This is known as static branch prediction. Another approach in which the prediction may change depending on execution history is called dynamic branch prediction.

23. List the two states in the dynamic branch prediction. (Remebering)

LT: Branch is likely to be taken.

LNT: Branch is likely not to be taken.

24. List out the four stages in the branch prediction algorithm. (Remebering)

ST : Strongly likely to be taken

LT : Likely to be taken

LNT : Likely not to be taken

SNT : Strongly not to be taken

25. List the features of the addressing mode used in the modern processor. (Remebering)

Access to an operand does not require more than one access to the memory.

- Only load and store instruction s access memory operand
- The addressing mode used does not have side effects.

26. Does the number of stages in the pipeline affect the performance?(Creating)

Yes. The number of pipeline stages will increase the speed of processing. It has one draw back. That is the probability of the pipeline being stall is also increased.

27. Give the advantages of complex addressing modes. (Remebering)

The main advantage of such modes is that they reduce the number of instructions needed to perform a given task and thereby reduce the program space needed in the main memory.

28. What is superscalar processor? (Understanding)

A processor capable of parallel instruction execution and having performance level greater than one instruction per cycle is known as **superscalar processor**.

29. What is register renaming? (Understanding)

When temporary register holds the contents of the permanent register the name of permanent register is given to that temporary register this is called **renaming.**

30.Explain the sequence to perform write operation. (Understanding)

- MAR⟶[R1]
- MDR⟶[R2]
- Wait for MFC

31.Explain cache hit and cache miss. (Understanding)

a. If the desired data are found in the cache ,that is referred to as **cache hit.**
b. If the desired data are not found in the cache ,that is referred to as **Cache miss.**

32. What are called stalls? (Understanding)

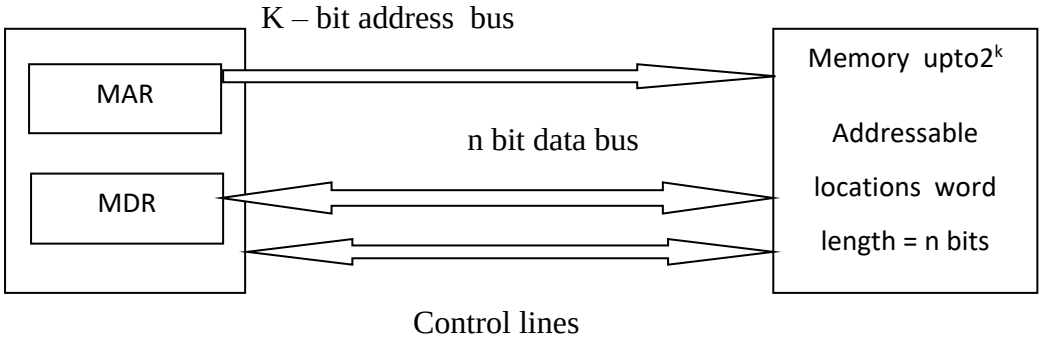
An alternative representation of the operation of a pipeline in the case of a cache miss gives the function performed by each pipeline stage in each clock cycle. The periods in which the decode unit, execute unit, and the write unit are idle are called stalls. They are also referred to as bubbles in the pipeline.

PART-B

1.Explain the various types of hazards in pipelining? **(Understanding)**
2.Write notes on super scalar operation? **(Applying)**
3.Explain the techniques used to overcome the various hazards. **(Understanding)**
4.Explain how pipelining helped to speedup the processor**(Understanding)**
5. Discuss the influence on instruction set.**(Applying)**
6.Describe about the performance considerations on pipeling in detail. **(Understanding)**
7.Explain the basic concept of pipelining(Four segment) with diagram and compare it with sequential processing. **(Understanding)**
8.Explain data hazard and how to deal with this problem. **(Understanding)**
9. What is branch hazard? Describe the methods for dealing with branch hazard? **(Understanding)**
10.Explain the function of a Six segment pipeline and Draw a space diagram. **(Understanding)**
11. What is Instruction hazard or Control hazard? Describe the methods for dealing it. **(Understanding)**
12. Describe about the Datapath and control considerations on pipeling in detail. **(Understanding)**

UNIT IV
MEMORY SYSTEM
PART-A
2 MARKS

1.How is memory connected to the processor?(Applying)



2. Define addressing scheme. (Understanding)

Addressing scheme is a scheme used in a ny computer to determine and maximum size of the memory.

3. What are the two registers involved in data transfer between the memory and the processor?

The registers used to transfer data are,

1. MAR (Memory address register)

2. MDR (Memory data register).

4. Define Memory access time. (Understanding)

A useful measure speed of memory units is the time that elapses between the initiation of an operation and the completion of that operation. This is referred to as memory access time.

5. Define Memory cycle time. (Understanding)

Memory cycle time is minimum time delay required between the initiation of to successive memory operations.

6. When is memory unit called as RAM?(Creating)

A memory unit is called as RAM if any location can be accessed for a read or writes operation in some fixed amount of time that is independent of the location address.

7.List out the RAM's types. (Understanding)

(i) Static RAM

(ii) Dynamic RAM

(a) Asynchronous DRAM

(b) Synchronous DRAM

8. What is cache memory? (Understanding)

Cache memory is a small, fast memory that is inserted between the larger, slower main memory and the processor.

9. What are the advantages of cache memory? (Understanding)

The advantages of cache memory are,

1. It reduces the Memory access time

2. It holds the currently active segments of a program and their data.

10.What is MMU?

MMU is the memory management unit. It is a special memory control circuit used for implementing the mapping of the virtual address space onto the physical memory.

11.List the Characteristics of Semiconductor RAM Memories.(Applying)

The semiconductor RAM memories has the following characteristics:

1.They are available in a wide range of speeds.

2.Their cycle times range from 100ns to less than 10ns.

3.They replaced the expensive magnetic core memories.

4.They are used for implementing memories.

12.Define Memory cell. (Understanding)

Memory cell is a cell which is usually organized in the form of an array in which each cell is capable of storing one bit of information.

13.What is a word line? (Understanding)

In a Memory cell,all the cells of a row are connected to a common line called as word line.

14.Define static memories.

Memories that consist of circuits capable of retaining their state as long as power is applied. It is called as static memories.

15.Difference between static RAM and Dynamic RAM.(Creating)

S.no	Static RAM	Dynamic RAM

1.	They are fast	They are slow
2.	They are very expensive	They are less expensive
3.	They require several transistors	They require less no several transistors
4.	They retain their state indefinitely	They do not retain their state indefinitely

16.Differentiate asynchronous DRAM with synchronous DRAM. (Creating)

S.no.	**asynchronous DRAM**	**synchronous DRAM**
1.	The timing of the memory device is controlled asynchronously	The timing of the memory device controlled synchronously.
2	There is specialized memory controlled circuit that provides the necessary control information	The memory operations are synchronized with a clock signals.
3	Separate refresh circuit is not used	It uses the separate refresh circuit.

17.Why SRAMS are said to be volatile?(Remebering)

Static RAMs are said to be volatile memories because their contents are lost when power is interrupted.

18.What is a refresh circuit? (Creating)

A refresh circuit is a circuit which ensures that the contents of a DRAM are maintained when each row of cells are accessed periodically.

19.What are asynchronous DRAMs? (Understanding)

In DRAM,the timing of the memory device is controlled asynchronously.A specialized memory controller circuit provides the necessary control signals RAS and CAS that govern the timing.The processor must take into account the delay in the response of the memory.Such memories are referred to as asynchronous DRAMs.

20.What are synchronous DRAMs? (Understanding)

Synchronous DRAMs are those whose operations is directly synchronized with a clock signal.

21.Define Memory latency. (Understanding)

Memory latency is used to refer to the amount of time it takes to transfer a word of data to or from the memory.

22.How can we achieve fast page mode operation in DRAM? (Understanding)

In DRAM we can apply a consecutive sequence of column addresses under the control of successive CAS signal. This allows transfers a block of data a much faster rate. This block transfer capability is referred as fast page mode.

23.What are CAS and RAS? (Understanding)

CAS and RAS are the two control signals used in DRAM to select the particular cell from the array of cells . CAS means column address strobe signals and RAS means Row address strobe signals.

24.Define memory bandwidth . (Understanding)

The number of bits or bytes that can be transferred in one second is known as memory bandwidth.

25.What is double data rate SDRAM? (Understanding)

The double data rate SDRAM can transfer data on both edges of the clock signals. So the bandwidth is doubled.

26.Define interleaving. (Understanding)

Cell array can be organized in two banks . Each bank can be accessed separately. So the consecutive words of given block are stored in different banks. It is known as interleaving of words. It increases the transfer rate.

27.How can you create large memory using dynamic memory system? (Understanding)

A large memory can be create by placing DRAM chips directly on the main system printed circuit board that contains the processor , often referred to as a mother board.

28. Define SIMM and DIMM. (Understanding)

SIMM - Single In – line memory modules .

DIMM - Dual In – line memory modules .

Theses two large memories are created by using the DRAM . This module is an assembly of several memory chips on a separate small board that plugs vertically into a single socket on the mother board.

29.What is RAMBUS Memory? (Understanding)

1. The key feature of Rambus technology is a fat signaling method used for transfer information between chips.

2. Instead of using signals that have voltage levels of either 0 or 5v to represent the logic values, rambus technology uses 0.3 and +2v.

30.What is Memory controller? (Understanding)

A memory controller is a circuit which is interposed between the processor and the dynamic memory. It is used for performing multiplexing of address bits.

31.Draw backs present in the DRAM.(Creating)

All dynamic memories have to be refreshed and it does not have a refreshing capability . So the memory controller has to provide all the information needed to control the refreshing operation. This increases the over head of the controller circuit.

32.Define Rambus DRAM. (Understanding)

It is specially designed memory chips. These chips use arrays based on the standard DRAM technology. Multiple banks of cell arrays are used to access more than one word at a time . Circuitry needed to interface to the rambus channel in included on the chip.

33.What is differential signaling and where we are using it? (Understanding)

Instead of using signals that have voltage levels of either 0 or V supply to represent logic values , the signals consist of much smaller voltage swings around a reference voltage Vref is used The reference voltage is about 2 V and two logic levels are represented by 0.3 V swings above and below V ref . This is type of signaling is known as differential signaling and it is used in rambus technology.

34.Define non volatile memory and given an example for it. (Understanding)

The non volatile memories can retain their contents if power is turned off.

Example for this memory is ROM which includes only the reading operation. ROM means read only memory . It can store booting information of the system.

35.What is meant by PROM and list out its advantages and disadvantages ? (Understanding)

PROM means programmable read only memory. It allows the data to be loaded by the user . It provides the flexibility and convenience not available with ROM.It allows the user to write the program only once.

36.Define EPROM. (Understanding)

EPROM means erasable programmable ROM. It allows the stored data to be erased and new data to be loaded. It uses the ultraviolet rays to erase the contents . Its contents can be erased and reprogrammed.

37.What is disadvantages involved in EPROM? (Understanding)

EPROM is that a chip must be physically removed from the circuit for reprogramming and that its entire contents are erased by the ultra violet light . It is not possible to remove the selective contents from EPROM

38.What are disadvantages in EEPROM? (Understanding)

The only difference of EEPROM is that different voltages are needed for erasing, writing, reading the stored data.

39.Define EEPROM. (Understanding)

EEPROM means erasable programmable electrically . It overcomes the drawbacks of the EPROM . It allows the user to erase the contents selectively . It uses the different voltage levels for erasing , writing and reading the stored data.

40.What is flash memory? (Understanding)

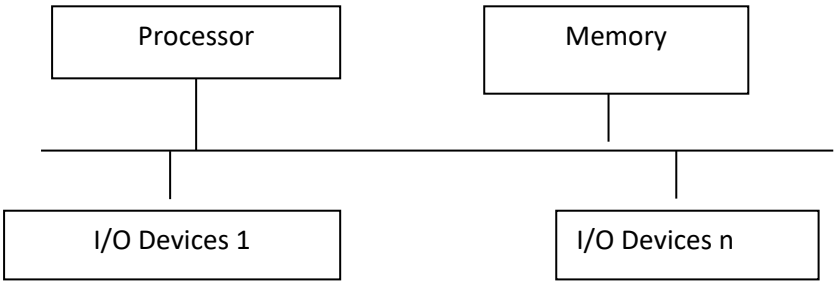
This is similar to flash memory . In EEPROM it is possible to read and write the contents of a single cell But in flash memory reading a single cell is possible but it is possible to write an entire block of cells.

PART-B

1. Write notes on semiconductor RAM memories. **(Understanding)**
2. Write notes on various types of ROMs. **(Understanding)**
3. What are the various types of cache mapping mechanisms? Explain in detail.
4. Write notes on secondary storage devices. **(Understanding)**
5. What are the various techniques used to improve the performance of cache. Explain it.
6. Explain with neat diagram the internal organization of bit cells in a memory chip. **(Understanding)**
7. Discuss the virtual memory management technique in detail **(Understanding)**
8. What is memory interleaving? Explain with neat diagram. **(Applying)**
9. Write brief notes on Optical Disks **(Understanding)**
10. Explain in detail Magnetic Hard Disks **(Understanding)**
11. What is virtual memory and explain how virtual address is translated into physical address? **(Understanding)**

UNIT V
I/O ORGANIZATION
PART-A
2 Marks

1. Give the organization of single bus structure. (Understanding)



2. What is memory mapped I/O? (Understanding)

With Memory mapped I/O, any machine instruction that can access memory can be used for transfer data to or from an I/O device.

3. What is program controlled I/O? (Understanding)

In program controlled I/O, the processor repeatedly checks a status flag to achieve the required synchronization between the processor and an input and output device.

4. What are the various mechanisms for implementing I/O operations ? (Understanding)

1. Program controlled I/O
2. Interrupts
3. Memory mapped I/O
4. DMA

5.Define ISR. (Understanding)

ISR means interrupt service routines . It can handle the execution of the interrupts and it responses to an interrupt request.

6.What constitute the device's interface circuit? (Understanding)

The address decoder, the data and status register and the control circuitry required to co-ordinate I/O transfers constitute the device's interface circuit.

7. What is interrupt service routine? (Understanding)

The routine executed in response to an interrupt request is called as interrupt service routine. In short ,it is called as ISR.

8. What is the purpose of interrupt acknowledgement signal? (Understanding)

The interrupt acknowledgement signal is used by the processor to inform the device that is request has been recognized so that it may remove its interrupt request signal.

9. Define interrupt latency. (Understanding)

The delay between the time an interrupt request is received and the start of execution of the interrupt service routine is called interrupt latency.

10. What is real time processing? (Understanding)

The concept of interrupts is used in many control applications where processing of certain routines must be accurately timed relative to external events. This type of application is called as real time processing?

11. What are Special gates used for driving INTR line? (Understanding)

The special gates used for driving INTR line are,

1.Open collector

2.Open drain

12.When is an interrupt line said to be edge – triggered? (Understanding)

An interrupt line is said to be edge triggered if the interrupt handling circuit responds only to the leading edge of the signal.

13.Give a typical scenario assuming that interrupts are enabled.(Applying)

A typical scenario as follows,

1. The device raises an interrupt request.
2. The processor interrupts the program currently being executed.
3. Interrupts are disabled by changing the control bits in the bus.
4. The device is informed that its request has been recognized and in response , it activates the interrupt request signal.
5. The action requested by the Interrupt is performed by the ISR.
6. Interrupts are enabled and execution of the interrupted program is resumed.

14.What are vectored interrupts? (Understanding)

To reduce the time involved in the polling process, a device requesting an interrupt may identify itself directly to the processor. Then the processor can immediately start executing the corresponding ISR.The term vectored interrupts refer to all interrupt handling schemes based on this approach.

15.What is interrupt vector? (Understanding)

Interrupt vector is the starting address of the interrupt service routine stored in the location pointed by the interrupting device.

16.What are privileged instructions? (Understanding)

Privileged instructions are the instructions which are executed only while the processor is running in the supervisor mode.

17.What is privilege exception? (Understanding)

An attempt to execute a privileged instruction while in the user mode leads to a special type of interrupt called a privilege exception.

18.What are the two independent mechanisms for controlling interrupt requests? (Understanding)

To control interrupt requests ,the mechanisms used are ,

1.At the device end , an interrupt enable bit in a control register determines whether the device is allowed to generate an interrupt request.

2.At the processor end, either an interrupt enable bit in the PS register or a priority structure determines whether a given interrupt request will be accepted.

19.What are exceptions? Give an Example? (Understanding)

An exception is a term often used to refer to any event that cause an interruption.

Eg. I/O interrupts.

20.What is a debugger? (Understanding)

A debugger is a program used by system software which helps the programmer finds errors in a program.

21.What are the two facilities provided by a debugger? (Understanding)

The facilities provided by a debugger are.

- 1.Trace
- 2.Breakpoints.

22.What does an exception occur when the processor is in trace mode? (Understanding)

When the processor is operating in the trace mode, an exception occurs after execution of every instruction, using the debugging program as the exception service routine. The trace exception is disabled during the execution of debugging program.

23.What are the uses of interrupts in OS? (Understanding)

The uses of interrupts in OS are,

- 1.To assign priorities
- 2.Switch from one user program to another.
- 3.Implementing security.
- 4.Protection features.
- 5.Co-ordinate I/O activities.

24.What is the process? (Understanding)

A program together with any information that describes current state of execution is regarded by the OS as an entity called process.

25.Define Multitasking. (Understanding)

Multitasking is a mode of operation in which a processor executes several user programs at the same time.

26.What is time slicing? (Understanding)

Time slicing is a common OS technique that makes multitasking possible. With this technique, each program runs for a short time period called as a time slice, then another program runs for its time slice and so on. The period, is determined by continuously running hardware clock, which generates an interrupt every seconds.

27.What are the three states of a process? (Understanding)

A process can be in one of the three possible states.

1.Running

2.Runnable.

3.Blocked.

28.Differenciate a process in running and runnable state.(Remebering)

The running state means that the program is currently being executed .The process is runnable if the program is ready for execution but is waiting to be selected by the scheduler.

29.What is program state? (Understanding)

A program state is state which includes register contents, program counter and the program status word.

30.What is DMA? (Understanding)

A special control unit that may be provided to allow transfer of a block of data directly between an external device and the main memory without continuous intervention by the processor. This approach is called Direct memory access.

31.What is the purpose of a DMA controller?

The DMA controller performs the functions that would normally be carried out by the processor when accessing the main memory.

32. What is cycle stealing? (Understanding)

Cycle stealing is an interweaving technique used by DMA controller to steal the memory cycles from the processor.

33.What is a block or burst mode? (Understanding)

The DMA controller may be given exclusive to the main memory to transfer a block of data without interruption. This is known as block or burst mode.

34.What is bus master? (Understanding)

The device that is allowed to initiate data transfers on the bus at any given time is called bus master.

35.What is bus arbitration? (Understanding)

Bus arbitration is the process by which the next device to become the bus master is selected and bus mastership is transferred to it.

36.Name the two approaches to bus arbitration. (Understanding)

The approaches to bus arbitration are,

1.Centralized arbitration

2.Distributed arbitration.

37.What do you mean by distributed arbitration? (Understanding)

Distributed arbitration means that all devices waiting to use the bus have equal responsibility in carrying out the arbitration process, without using a central arbiter.

38.What is the purpose of a bus protocol? (Understanding)

A bus protocol is the set of rules that governs the behavior of various devices connected to the bus.

39.Define master. (Understanding)

Master is a device that initiates data transfer by issuing read or write commands on the bus. Master is also called as initiator.

39.What is a slave. (Understanding)

The device addressed by the master is called as slave. Slave can also called as target.

40.What is a synchronous bus? (Understanding)

In synchronous bus , all devices derive timing information from the common clock line. Equally spaced pulses on this define equal time intervals.

41.What is the difference between serial port and parallel port? (Understanding)

1.A parallel port transfers data in the form of a number of bits typically 8 or 16 simultaneously to or from the device.

42.What is a bridge?(Creating)

A bridge is an interconnection circuit between two buses. It translates the signals and protocols of one bus into those of the other.

43.What is transaction? (Understanding)

A complete transfer operation on the bus , involving an address and a burst of data is called a transaction.

44.Define SCSI. (Understanding)

SCSI stands for small computer system interface. It refers to a standard bus defined by ANSI under designation X3.131.

45.What are the different categories of SCSI bus signals? (Understanding)

SCSI bus signals are classified as,

1.Data signal

2.Phase signal

3.Information signal

4.Handshake.

5.Direction of transfer.

46.What are the objectives of USB? (Understanding)

The objectives of USB are as follows,

1.Provide a simple ,low cost and easy to use interconnection system.

2.Enhance user convenience through a 'plug and play' mode operation.

47.What is isochronous? (Understanding)

An isochronous data stream means that the successive events are separated by equal periods of time.

48.What is hub? (Understanding)

A hub is the intermediate control point between the host and the I/O device.

49.Define serial port. (Understanding)

A serial port transmits and receives data one word bit at a time.

PART-B

1.Explain the various methods available to handle multiple devices using interrupts? **(Understanding)**

2. Write notes on interrupts in operating system? **(Applying)**

3. Explain DMA and the different types of bus arbitration mechanisms. **(Understanding)**

4. Explain the accessing of I/O devices. **(Understanding**

5. Explain Synchronous and Asynchronous bus. **(Understanding)**

6. Explain the Interface circuits. **(Understanding)**

7. Explain the Peripheral Component Interconnect (PCI) Bus. **(Understanding)**

8. Explain the SCSI Bus. **(Understanding)**

9. Explain Universal Serial Bus (USB). **(Understanding)**