Permission Letter

From

Mr.A.VELLIANGIRI & Mr.J.RAMESH KUMAR
Assistant Professor,
Department of ECE,
K.S.R. College of Engineering,
Tiruchengode - 637 215

To

The Principal,
K.S.R. College of Engineering,
Tiruchengode – 637 215

Respected Sir,

Sub: Webinar on **"Low Power VLSI"** - Permission requested - Reg.

The ECE department has planned to conduct a Free Webinar on **"Low Power VLSI"** sponsored by NoviTech on **29.08.2020 at 04.00 PM**. We request you to grant permission to conduct the Webinar.

Thanking You

Date: 20.08.2020

Place: Tiruchengode

Yours sincerely,

K.S.R College of Engineering (Autonomous), TIRUCHENGODE-637215

Department OF Electronics and Communication Engineering

Webinar on "LOW POWER VLSI"

Convener
Dr.P.S.Periasamy
Professor & Head, Dept. of ECE
Coordinator
Mr. A . Velliangiri, AP/ECE Dr.P.Mahendran, AP/ECE Mr.J.Rameshkumar, AP/ECE

Date : 29/08/2020 **Time : 4.00pm to 5.00pm**

Tamilnadu | Kerala +91-9489822548
+91-97467 42936

Registration Link : https://bit.ly/3dfmMgU

in association with NoviTech on 29.08.2020 at 4.00 PM through you tube link https://youtu.be/9R5SnNKw_nI

K.S.R COLLEGE OF ENGINEERIG (Autonomous), TIRUCHENGODE-637215

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NOVITECH FREE WEBINAR ON "LOW POWER VLSI"

01.09.2020

WEBINAR REPORT

Department of Electronics and Communication Engineering, K.S.R College of Engineering (Autonomous), Tiruchengode Organized a Webinar on "LOW POWER VLSI" in association with NoviTech on **29.08.2020 at 4.00 PM** through you tube link https://youtu.be/9R5SnNKw_nI.

The Webinar began with welcome address by **Dr. P. S. Periasamy** the Head of the Department, ECE. He introduced the resource person **Mr. Thirumalai, NoviTech**, to deliver the lecture and welcomed all the participants.

Impact Analysis on Webinar

- The webinar was very useful to the Faculty members and students to learn about the fundamentals of Low Power VLSI. It was very useful for gaining knowledge regarding **Design and Simulation of Combinational logic circuits using Tanner EDA Tool**. The lecture was even more interesting with the **Tanner EDA Tool LIVE** demonstrations.
- This webinar helped the Faculty members and students to improve their knowledge on the field of Low Power VLSI and the students may have the opportunity to participate in more workshops.
- The webinar has also motivated the students to do more projects using sensors for Low Power VLSI applications. **156 participants** were attended the webinar successfully.

Impacts on Programme Outcomes:

PO1-Engineering Knowledge:

This webinar provides basic engineering knowledge on Low Power VLSI.

PO3 - Design/development of solutions:

This webinar helps to Design and Simulation of Combinational logic circuits using Tanner EDA Tool.

PO11-Project Management and finance:

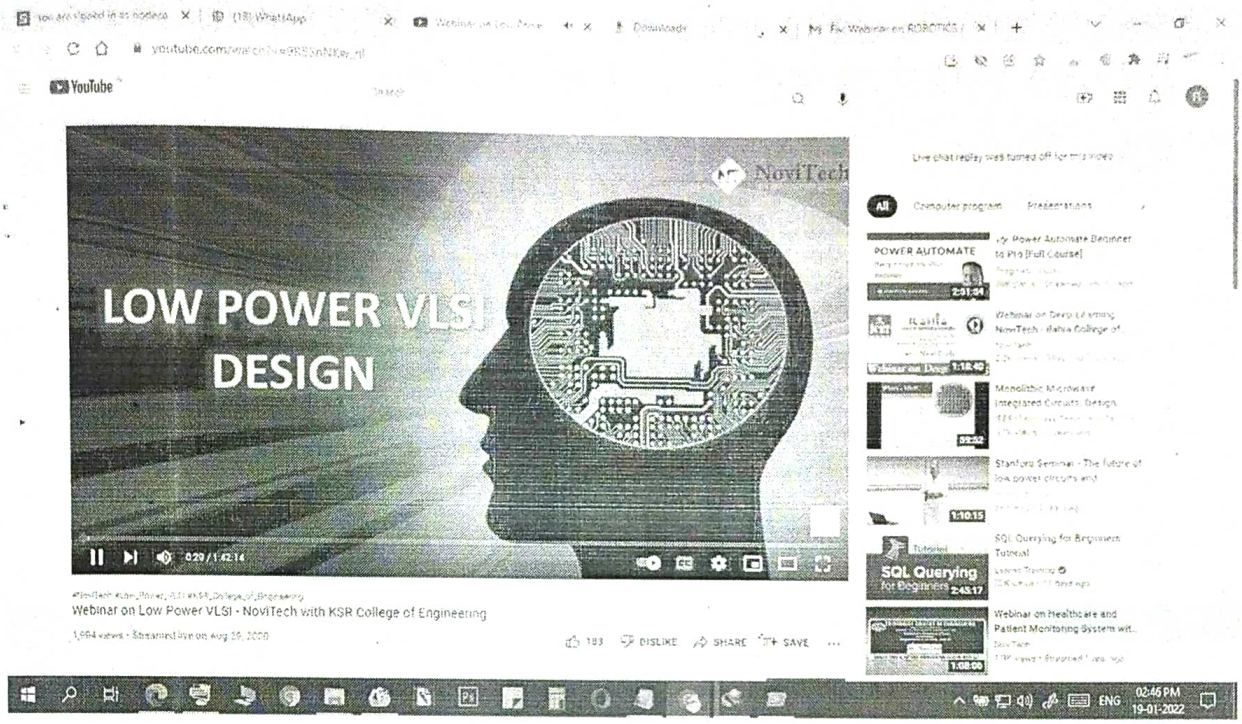
This webinar motivated many of the students to do project on Low Power VLSI

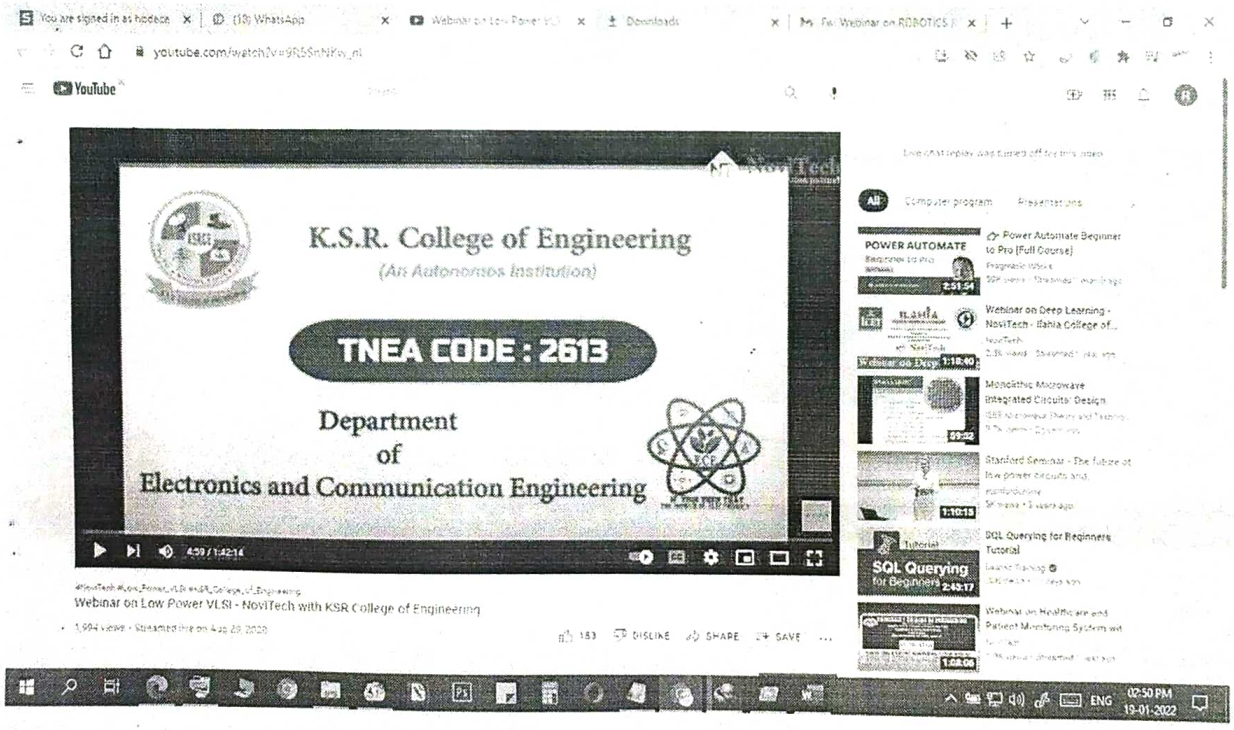
PO12-Life-long Learning:

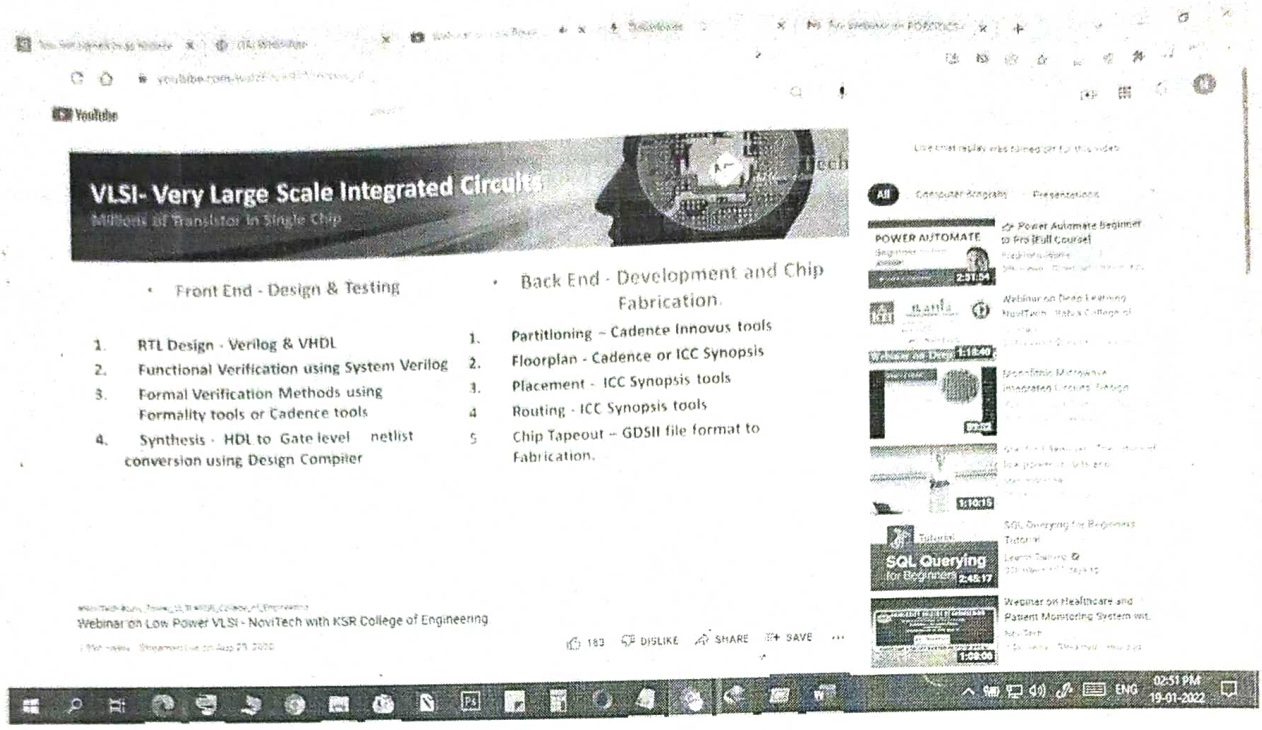
This webinar provides information on Power gating and Clock gating methods using DSCH and Tanner EDA hence helps life-long learning.

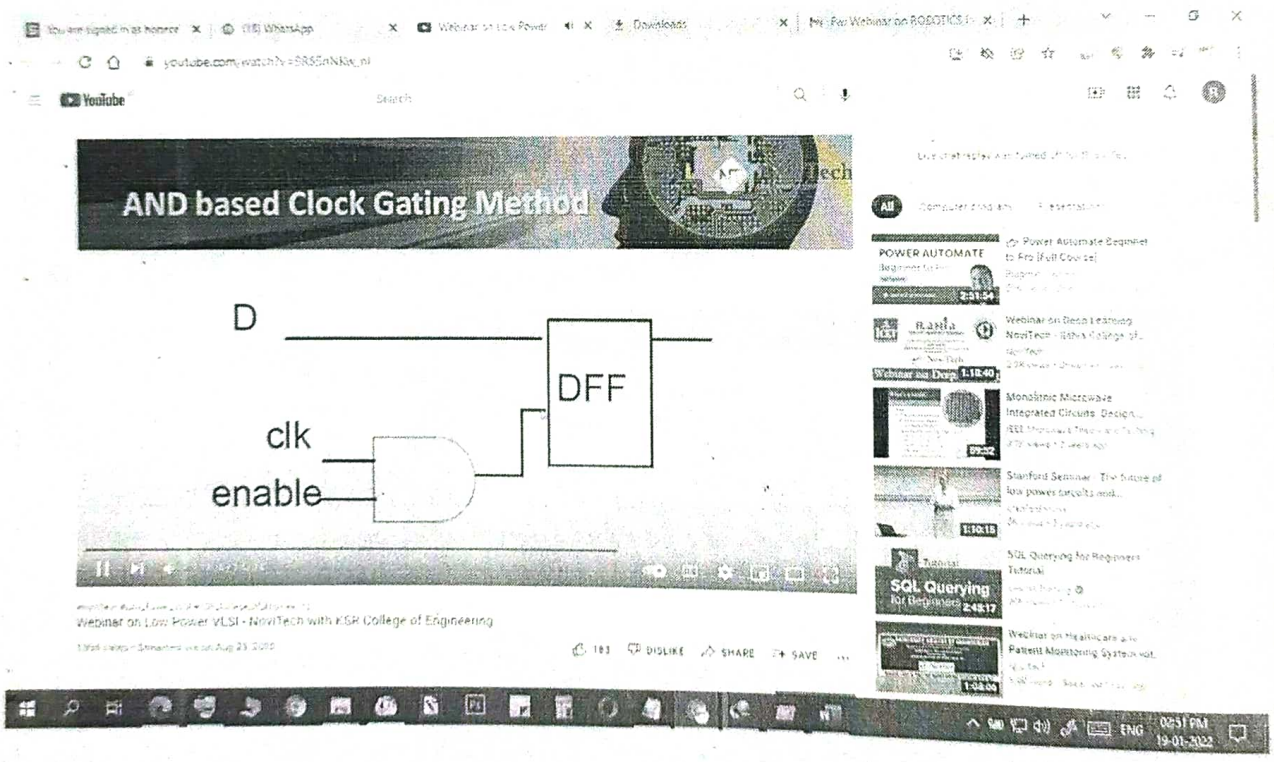
Information Brochure

SCREEN SHOTS









Coordina
[Dr. P.S.PERIASA