

Permission Letter

From

Mr.A.VELLIANGIRI & Mr.J.RAMESH KUMAR

Assistant Professor,

Department of ECE,

K.S.R. College of Engineering,

Tiruchengode - 637 215

To

The Principal,

K.S.R. College of Engineering,

Tiruchengode – 637 215

Respected Sir,

Sub: Webinar on “**Low Power VLSI**” - Permission requested - Reg.

The ECE department has planned to conduct a Free Webinar on “**Low Power VLSI**” sponsored by NoviTech on **29.08.2020 at 04.00 PM**. We request you to grant permission to conduct the Webinar.

Thanking You

Date: 20.08.2020

Place: Tiruchengode



Yours sincerely,



K.S.R College of Engineering (Autonomous), TIRUCHENGODE-
637215

Department OF Electronics and Communication Engineering

Webinar on **"LOW POWER VLSI"**



K.S.R.
COLLEGE OF ENGINEERING

(An Autonomous Institution)
K.S.R. Kalvi Nagar, Tiruchengode – 637 215,
Tamil Nadu, India

DEPARTMENT

OF
ELECTRONICS AND COMMUNICATION ENGINEERING

ORGANIZES

WEBINAR ON

Low Power VLSI

in Association with



NoviTech
the innovation partner

Convener

Dr.P.S.Periasamy

Professor & Head, Dept. of ECE

Coordinator

Mr. A . Velliangiri, AP/ECE

Dr.P.Mahendran, AP/ECE

Mr.J.Rameshkumar, AP/ECE



Date : 29/08/2020



Time : 4.00pm to 5.00pm

Tamilnadu | Kerala

+91-9489822548

+91-97467 42936

Registration Link : <https://bit.ly/3dfmMgU>



in association with NoviTech on 29.08.2020 at 4.00 PM through you
tube link https://youtu.be/9R5SnNKw_nI

K.S.R COLLEGE OF ENGINEERING (Autonomous), TIRUCHENGODE-637215
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NOVITECH FREE WEBINAR ON "LOW POWER VLSI"

01.09.2020

WEBINAR REPORT

Department of Electronics and Communication Engineering, K.S.R College of Engineering (Autonomous), Tiruchengode Organized a Webinar on "LOW POWER VLSI" in association with NoviTech on **29.08.2020 at 4.00 PM** through you tube link https://youtu.be/9R5SnNKw_nI.

The Webinar began with welcome address by **Dr. P. S. Periasamy** the Head of the Department, ECE. He introduced the resource person **Mr. Thirumalai, NoviTech**, to deliver the lecture and welcomed all the participants.

Impact Analysis on Webinar

- The webinar was very useful to the Faculty members and students to learn about the fundamentals of Low Power VLSI. It was very useful for gaining knowledge regarding **Design and Simulation of Combinational logic circuits using Tanner EDA Tool**. The lecture was even more interesting with the **Tanner EDA Tool LIVE** demonstrations.
- This webinar helped the Faculty members and students to improve their knowledge on the field of Low Power VLSI and the students may have the opportunity to participate in more workshops.
- The webinar has also motivated the students to do more projects using sensors for Low Power VLSI applications. **156 participants** were attended the webinar successfully.

Impacts on Programme Outcomes:

PO1-Engineering Knowledge:

This webinar provides basic engineering knowledge on Low Power VLSI.

PO3 - Design/development of solutions:

This webinar helps to Design and Simulation of Combinational logic circuits using Tanner EDA Tool.

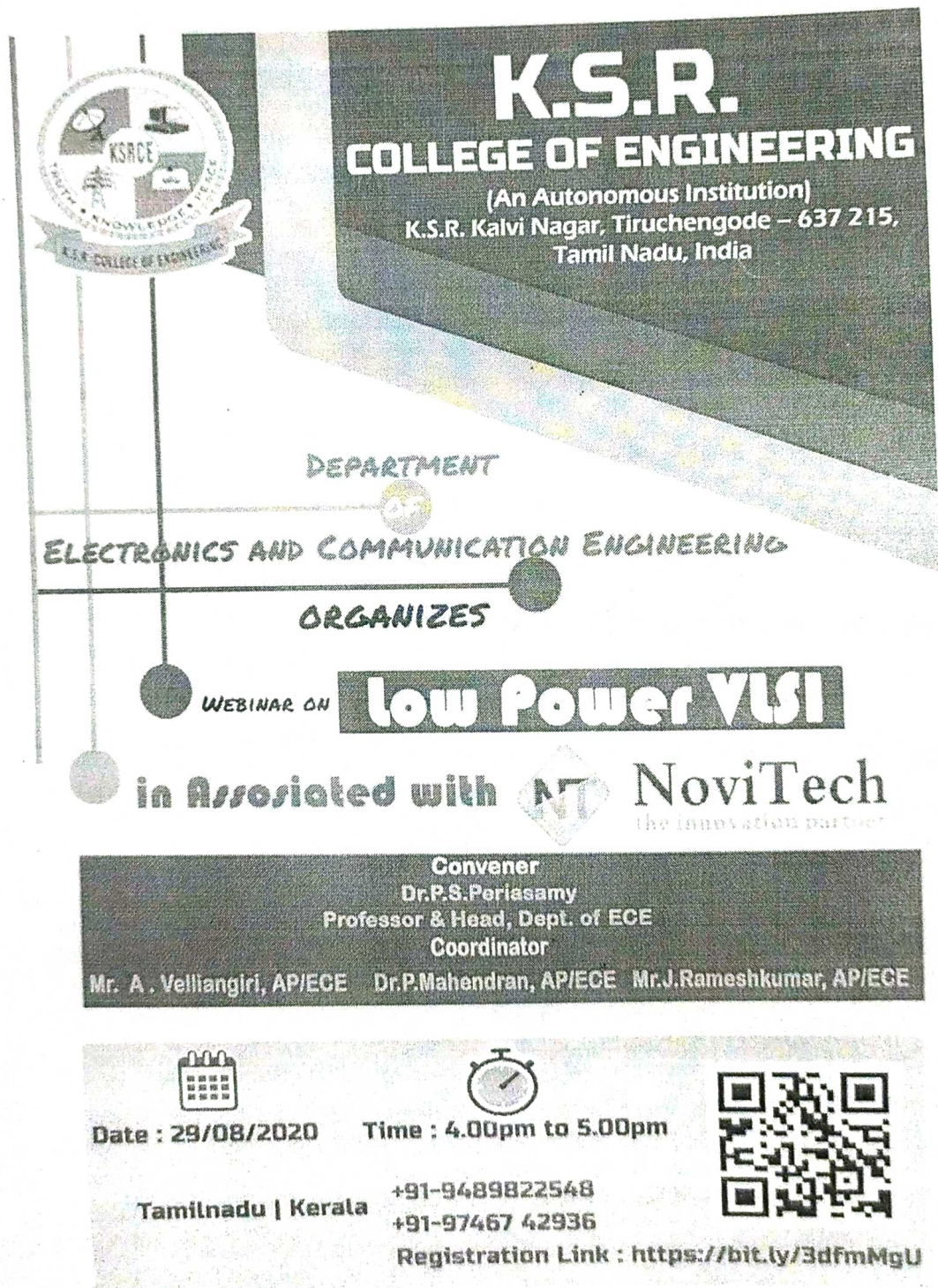
PO11-Project Management and finance:

This webinar motivated many of the students to do project on Low Power VLSI

PO12-Life-long Learning:

This webinar provides information on Power gating and Clock gating methods using DSCH and Tanner EDA hence helps life-long learning.

Information Brochure



The brochure features a grid layout with a vertical line on the left and horizontal lines intersecting it. The K.S.R. College of Engineering logo is at the top left. The text 'K.S.R. COLLEGE OF ENGINEERING' is prominently displayed in a large, bold font. Below it, the college's address is listed. The word 'DEPARTMENT' is written above 'ELECTRONICS AND COMMUNICATION ENGINEERING'. The word 'ORGANIZES' is written below the department name. The text 'WEBINAR ON' is written above 'Low Power VLSI'. The phrase 'in Associated with' is written above the NoviTech logo. The NoviTech logo is a stylized 'NT' inside a diamond shape. Below the NoviTech logo, the text 'the innovation partner' is written. The names of the convener and coordinator are listed in a box. The date and time of the webinar are listed in a box. The contact information for the college is listed in a box. A QR code is located at the bottom right of the brochure.

K.S.R.
COLLEGE OF ENGINEERING
(An Autonomous Institution)
K.S.R. Kalvi Nagar, Tiruchengode – 637 215,
Tamil Nadu, India

DEPARTMENT
ELECTRONICS AND COMMUNICATION ENGINEERING

ORGANIZES

WEBINAR ON **Low Power VLSI**

in Associated with **NoviTech**
the innovation partner

Convener
Dr.P.S.Periasamy
Professor & Head, Dept. of ECE
Coordinator
Mr. A . Velliangiri, AP/ECE Dr.P.Mahendran, AP/ECE Mr.J.Rameshkumar, AP/ECE

Date : 29/08/2020 **Time : 4.00pm to 5.00pm**

Tamilnadu | Kerala **+91-9489822548**
+91-97467 42936
Registration Link : <https://bit.ly/3dfmMgU>

SCREEN SHOTS

YouTube video player interface showing a video titled "LOW POWER VLSI DESIGN". The video is from the channel "NoviTech" and has 1,594 views. The video player shows a progress bar at 0:29 / 1:42:14. The video content features a silhouette of a head with a circuit board inside, and the text "LOW POWER VLSI DESIGN".

Below the video player, the video title "Webinar on Low Power VLSI - NoviTech with KSR College of Engineering" is displayed, along with the view count and upload date "1,594 views · Streamed live on Aug 25, 2022".

The right sidebar shows a list of recommended videos, including "POWER AUTOMATE", "Webinar on Deep Learning", "Monolithic Microwave Integrated Circuits Design", "Standard Seminar - The future of low power circuits and", "SQL Querying for Beginners", and "Webinar on Healthcare and Patient Monitoring System".

The Windows taskbar at the bottom shows the system clock as 02:46 PM on 19-01-2022.

YouTube video player interface showing a video titled "K.S.R. College of Engineering (An Autonomous Institution) TNEA CODE : 2613 Department of Electronics and Communication Engineering". The video is from the channel "NoviTech" and has 1,594 views. The video player shows a progress bar at 4:59 / 1:42:14. The video content features the college logo and the text "K.S.R. College of Engineering (An Autonomous Institution) TNEA CODE : 2613 Department of Electronics and Communication Engineering".

Below the video player, the video title "Webinar on Low Power VLSI - NoviTech with KSR College of Engineering" is displayed, along with the view count and upload date "1,594 views · Streamed live on Aug 25, 2022".

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The Windows taskbar at the bottom shows the system clock as 02:50 PM on 19-01-2022.

YouTube

VLSI- Very Large Scale Integrated Circuits

Millions of Transistor in Single Chip

Front End - Design & Testing

1. RTL Design - Verilog & VHDL
2. Functional Verification using System Verilog
3. Formal Verification Methods using Formality tools or Cadence tools
4. Synthesis - HDL to Gate level netlist conversion using Design Compiler

Back End - Development and Chip Fabrication.

1. Partitioning - Cadence Innovus tools
2. Floorplan - Cadence or ICC Synopsis
3. Placement - ICC Synopsis tools
4. Routing - ICC Synopsis tools
5. Chip Tapeout - GDSII file format to Fabrication.

Webinar on Low Power VLSI - NovTech with KSR College of Engineering

139 views · Streamed live on Aug 23, 2022

183 DISLIKE SHARE SAVE

02:51 PM 19-01-2022

YouTube

AND based Clock Gating Method

Webinar on Low Power VLSI - NovTech with KSR College of Engineering

139 views · Streamed live on Aug 23, 2022

183 DISLIKE SHARE SAVE

02:51 PM 19-01-2022

[Signature]

Coordinating
[Dr. P.S.PERIASAN]