

# **K.S.R. COLLEGE OF ENGINEERING (Autonomous),TIRUCHENGODE – 637 215.**

## **DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

### **FACULTY PROFILE**

- 01. Name : USHA P**
- 02. Designation : ASSISTANT PROFESSOR**
- 03. Date of Birth : 27.03.1993**
- 04. Date of Joining : 01.07.2020**



**05. Qualification & Designation :**

	<b>At the time of Joining</b>	<b>Now</b>
<b>Qualification</b>	M.E	M.E
<b>Designation</b>	Assistant Professor	Assistant Professor

- 06. Specialization : VLSI Design**
- 07. Area of Interest : Digital Electronics and VLSI Design**
- 08. Experience & Promotion Details (Chronological):**

<b>SL.NO.</b>	<b>Name of the Organization</b>	<b>Designation</b>	<b>Period</b>	
			<b>From</b>	<b>To</b>
1	AKT Memorial College of Engineering and Technology	Assistant Professor	24.08.2016	23.06.2018
2	K.S.R. College of Engineering	Assistant Professor	18.07.2018	Till date

**09. Publication Details:-**

	<b>*National Level</b>		<b>*International Level</b>	
	<b>Journal(s)</b>	<b>Conference(s)</b>	<b>Journal(s)</b>	<b>Conference(s)</b>
Others	-	-	01	01

**10. Details of Workshops/ Seminars/Webinar Attended**

1. Attended a Seminar on Digital Signal Processing and its Application held at Sri Ramakrishna Institute of Technology, Coimbatore.
2. Attended a one day Workshop on Embedded System design using 8051 Microcontroller, held at PGP college of Engineering and Technology, Namakkal.
3. Attended a three days National Level Workshop on Embedded C held, at Selvam College of Technology, Namakkal.

**11. Details of the Subjects Handled:**

Sl.No	Academic Year	Semesters	Name of the Subject	Class	% of Pass
1)	2015-2016	Odd	Digital Electronics	II ECE	83.00
2)	2016-2017	Even	VLSI Design	III ECE	78.00
3)	2017-2018	Odd	Digital Electronics	II ECE	80.00
4)	2018-2019	Even	VLSI Design	IV ECE	75.00
5)	2019-2020	Even	Cryptography and Network Security	IV ECE	90.00
6)	2020-2021	Odd	C++ and Data structures	II ECE	80.00
7)	2021-2022	Even	Cryptography and Network Security	IV ECE	100

**15. Additional Responsibilities: -**

SL.NO	Details of Work	Work allotted by	Duration
1.	VLSI Lab Incharge	Head of the Department	2016-2018
2.	Student Mentor	Head of the Department	2018 to Till Date

**Signature****Annexure****LIST OF PUBLICATIONS****International Conference: 01**

1.P.Usha” Design and Analysis of Combinational Circuits Using Gate Diffusion Input”,  
Second International Conference on Electrical, Electronics and Computer  
Engineering”, Vivekanandha College of Engineering for Women, Tiruchengode.

**JOURNAL PUBLICATIONS:****International Journal:01**

1.P.Usha, “Design and Analysis of Combinational Circuits Using Gate Diffusion Input”,  
“CiiT Software and Engineering Technology”, Volume 08, Issue 1, PP 5-10, Feb 2016.