

K S R COLLEGE OF ENGINEERING, TIRUCHENGODE

(Autonomous)

Approved by AICTE, New Delhi & Affiliated to Anna University

Chennai

ORGANIZED BY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

WEBINAR

ACADEMIC YEAR: 2020-2021

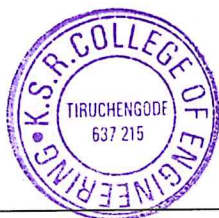
TITLE

“LOW POWER VLSI IN ASSOCIATED WITH NOVI TECH”

on

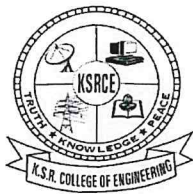
29.08.2020

Co-ordinator: Mr.A.Velliangiri,AP/ECE



A handwritten signature in green ink, likely belonging to the Principal, is positioned above the printed name.

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TIRUCHENGODE-637 215**



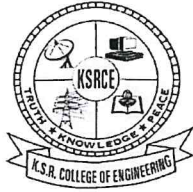
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Event Schedule

1	Name of the Event (Seminar/Workshop/Conference/FDP/Any other)	webinar
2	Name of the Organizer	Electronics and communication Engineering
3	Date of Event	29.08.2020
4	Platform	Online mode
5	Title of the Event	Webinar on Low power VLSI
6	Name of the Coordinator	Mr.A. Vellingiri
7	Total Participants	156
8	Objectives of the Event	To make student a better understanding of trends in technologies in emerging VLSI technology, the circuit complexity and high speed imply significant increase in the power consumption




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REPORT OF THE PROGRAM

Intent of the webinar

The Webinar titled "Low Power VLSI" broaden the student skills, as well as their understanding of their field of interest. This also allows students to attain new knowledge and skills that can complement their main field of study.

Theme of the webinar

Department of Electronics and Communication Engineering organized a webinar in association with Novitech on August 29, 2020 through online mode. Mr. Thirumalai, NoviTech, coimbatore, hosted the webinar, which had 156 participants.

The aim of conducting this webinar titled "Low power VLSI" is to minimise the individual components as much as possible hence decreasing the total power consumption. Switching and short circuit power make up the dynamic power, whereas leakage current that passes through a transistor make up the static power.

Topics covered

The program is organized in such way that the participants start with learning about VLSI Technology, recent trends and applications. The following topics were discussed in the webinar. They are listed below,

- Introduction to VLSI
- Front End – Design and Testing
- Back End – Development and chip fabrication
- Modes of Logic Circuits
- Types of Power Dissipation
- Cloning and Decoding Gated Clocks
- Power estimation methods and Tools
- Power Reduction in Processors

CO-ORDINATOR



HOD/ECE

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Permission Letter

From

Mr.A.VELLIANGIRI & Mr.J.RAMESH KUMAR

Assistant Professor,

Department of ECE,

K.S.R. College of Engineering,

Tiruchengode - 637 215

To

The Principal,

K.S.R. College of Engineering,

Tiruchengode – 637 215

Respected Sir,

Sub: Webinar on “**Low Power VLSI**” - Permission requested - Reg.

The ECE department has planned to conduct a Free Webinar on “**Low Power VLSI**” sponsored by NoviTech on **29.08.2020 at 04.00 PM**. We request you to grant permission to conduct the Webinar.

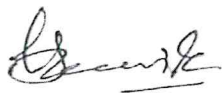
Thanking You

Date: 20.08.2020

Place: Tiruchengode



Yours sincerely,



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Tamil Nadu, India

DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

ORGANIZES

WEBINAR ON

Low Power VLSI

in Association with



NoviTech
the innovation partner

Convener

Dr.P.S.Periasamy

Professor & Head, Dept. of ECE

Coordinator

Mr. A . Velliangiri, AP/ECE Dr.P.Mahendran, AP/ECE Mr.J.Rameshkumar, AP/ECE



Date : 29/08/2020



Time : 4.00pm to 5.00pm

Tamilnadu | Kerala



91-9489822548

+91-97467 42936

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Registration Link: <https://bit.ly/3dfmMgU>

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youtube.com/watch?v=9R55nNKw_nI

YouTube

LOW POWER VLSI DESIGN

NoviTech

Webinar on Low Power VLSI - NoviTech with KSR College of Engineering

1,394 views • Streamed live on Aug 29, 2020

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TNEA CODE : 2613

Department of
Electronics and Communication Engineering

NoviTech

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Search

VLSI- Very Large Scale Integrated Circuits

Millions of Transistor in Single Chip

- Front End - Design & Testing
 1. RTL Design - Verilog & VHDL
 2. Functional Verification using System Verilog
 3. Formal Verification Methods using Formality tools or Cadence tools
 4. Synthesis - HDL to Gate level netlist conversion using Design Compiler
- Back End - Development and Chip Fabrication.
 1. Partitioning - Cadence Innovus tools
 2. Floorplan - Cadence or ICC Synopsis
 3. Placement - ICC Synopsis tools
 4. Routing - ICC Synopsis tools
 5. Chip Tapeout - GDSII file format to Fabrication.

Webinar on Low Power VLSI - NoviTech with KSR College of Engineering

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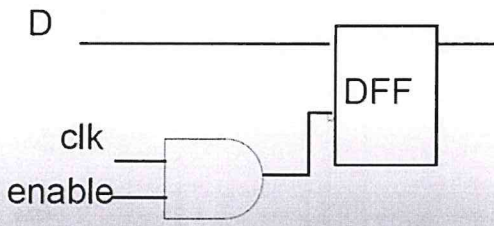
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youtube.com/watch?v=9R55nNKw_nI

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AND based Clock Gating Method



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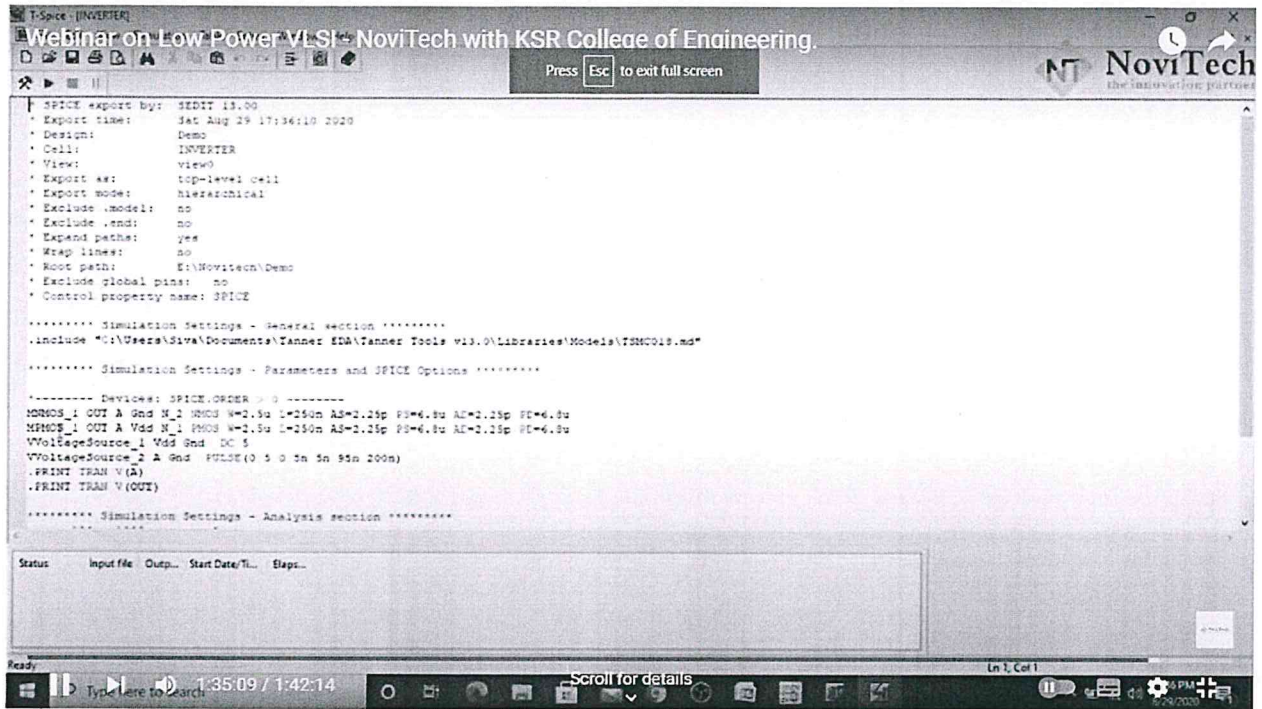
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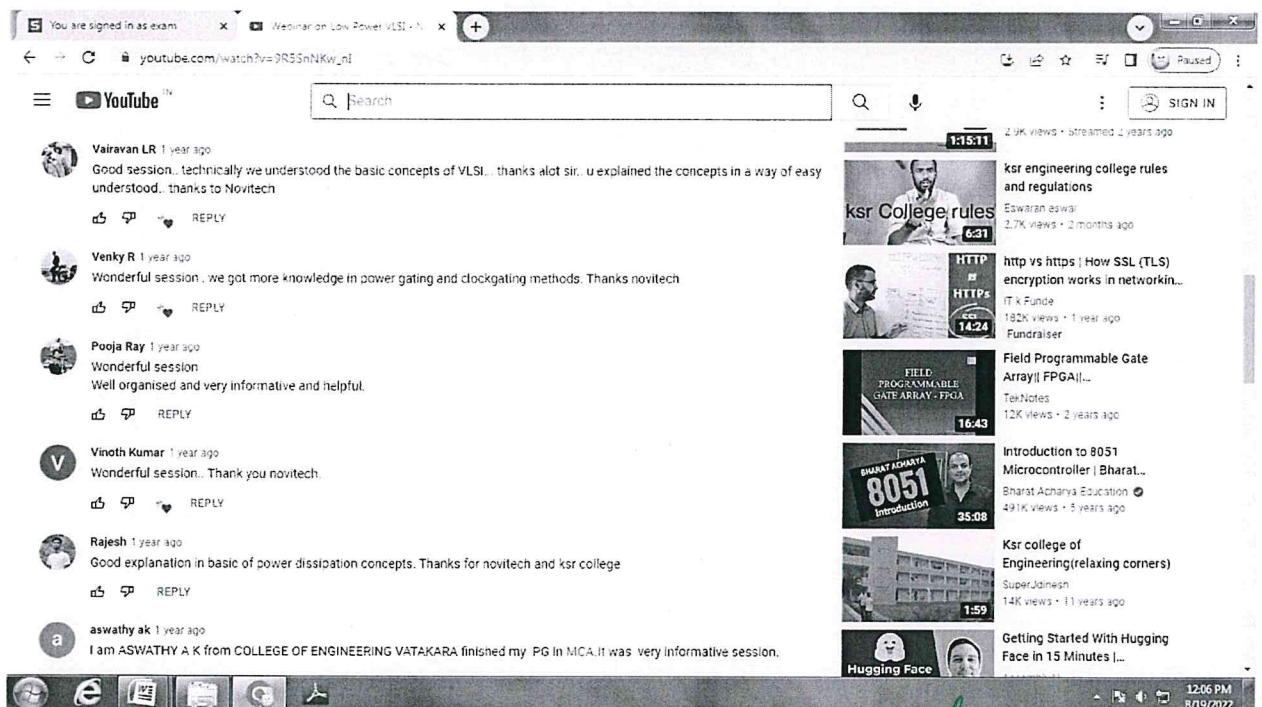
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Feedback of the participants



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YouTube interface showing a video player and comments. The video title is "Webinar on Low Power VLSI". The comments section shows several user comments, including one from BISHAL SARKAR and another from AVANI S K. The video player shows a thumbnail for "EUV: Lasers, plasma, and the sci-fi tech that will make chips..." with a duration of 1:00:05.

Comments:

- BISHAL SARKAR 1 year ago
Feedback: Excellent explanation with real time demo
Name: Mr. Bishal Sarkar
College: Hindustan University
Dept: M.tech E.C.E
Specialisation: Embedded and Real Time System
Show less
- AVANI S K 1 year ago
This was a good session.
AVANI S K,
ECE department,
M G COLLEGE OF ENGINEERING,VANDITHADAM
- Muthu Suba 1 year ago
Nice.. keep going Novitech
- MURUGAN.C 1 year ago
Good session. Thanks novitech.

Video Player:

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